

Fabrication of Silicon VLSI Circuits
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IIT Bombay
Lecture No. 1
Introduction Micro to Nano
A Journey into Integrated Circuit Technology

This course as I said is something to do with current technologies going on, so I just want to tell you that this course requires understanding or at least some clever or some interest in physics, chemistry, maths, material science mechanical, civilian, electrical any branch of engineering and actually that is how I like the area because I myself have fabricated the first India chip along with others in (()) (0:43).

So we are the first already called pioneers in making India's first chip in 1979-80. So (()) (0:52) not have actually given us impetus to work in this area and you need to know many things. So actually a technology should not be taught technology should be actually done then why this course? The course probably is before you enter the lab these days the technology has become so complex that unless you have priory values known of what to do in the lab which says simulations, process simulations.

Unless you do all over certain design by (()) (1:23) on a computer we should not enter the lab because things can go array if you have no idea where to work with, okay. So this course essentially is trying to, we will see what is my objective and as I say ATS down the line I mean many years ago I taught, my other students has joined as faculty now they are professors and they have been actually wanting to teach this course Ram Gopal Rao for example.

He joined in 96-98 and he say's I would like to teach this course I said take it then I started a course analogue circuits VLSI analogue than some other person joined and she said I want to teach analogue I said take it. Then I started a course called RF design RF VLSI then they said some other person Shalap Gupta aim and then they said no, sir I want to teach I said take it. So now I have nothing left to, I have started 5 new courses in this group but somehow I was not allowed to continue for long and Miri accept this technology which I taught 16 years at that trot, okay.

So it is a pleasure for me to come back to area which is most what I should say, the area which I like most but in IIT last for some years now people think I am in circuits, yes I am doing VLSI design for last maybe 20 years simply because in India the VLSI industry is mostly (()) (2:57) industry there are no fabs and therefore the students find it very easy to have a design project or design knowledge to get absorbed during this (()) (3:07) which relate really much higher pay scales than any other branch of engineering maybe except the computer science. So this is how we kept working on VLSI design activities, so even those courses which I started N people have started taking that course so I am left with teaching second years.

Okay, so I teach analogue, digital devices to second years, so after many years (()) (3:35) did page to your Sego Cmos VLSI design for Mtech that was the last Mtech course I had. Hopefully this maybe not the last maybe they will give me another one, you know after you retire and your chair is not there no one cares, okay. So that is my problem due regards to all of my colleagues.

So this area as I say, today maybe on Friday I will only introduce to you what is going on in the world some kind of history of electronics or history of semiconductors and please take it, this is a sentence I keep repeating every year with no good results many a times, those who forget history, history forgets them faster, okay. So never leave your history because history is the only thing which is linked to you for future.

Another value that I found that this year, for last 3 years one of my student is now Professor Anil was taking this course and I gradually asked him a few days ago, how many students he was having in last 3 years he said 85 to 90, I said fine that is a great number, 85 to 90 is a big number. Today morning unfortunately I just opened the webpage for this course I saw 150 was dazed, second day I understand 150.

Okay, so as I say for the last 2 years I am retired and maybe another 3 years I may stay hopefully. So this is a course which I like the most and have not taught many years, so let us see I do justice to what I understand and what you understand.

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VLSI Technology: EE 669, Autumn 2014

- Professor: Prof. A.N.Chandorkar,
EE Dept Office
- Email: anc@ee.iitb.ac.in
- Class Time: 11:05 AM – 12:35 PM
- Class Hrs: Wednesday and Friday (GG 401: CDEEP studio)
- Credits: 6 credits
- Objectives:
 - To expose students to a Technology which has revolutionized the world in every sphere. The Course emphasizes on Silicon Integrated Circuit technology and presents a detailed information on various Processes which allows Silicon ICs to function as desired Electronic system.
 - Modeling and Techniques of various Fabrication process are discussed with reference to realization CAD based Process design.
 - A brief introduction to processes in realization of silicon Solar cells will also be part of this course.

Course Text & Materials:

1. J.D.Plummer, M.D.Deal, and P.B. Griffin, "Silicon VLSI Technology: Fundamentals, Practice and Modeling", Prentice Hall Electronics and VLSI Series, Second Edition.
2. Sorab K. Ghandhi, "VLSI Fabrication Principles", Wiley Interscience.
3. F. Chang and S.M.Sze, "ULSI Technology", McGraw Hill

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Here is something details about this course, my name of course is there, my email address you write down, it is a 6 credit goals and my objective for the course is to expose you all to a technology which has revolutionised and the world in every sphere of our life. The course emphasises on silicon integrated circuit, so there are many other semiconductors which are becoming more popular now hopefully they may also later joined the pace but today of course it is silicon, silicon and silicon.

So we will talk only about silicon IC fab and will try to give you enough information on various processes which are used in fabricating these ICs. Major threat will be modelling up processors and also we will give you what are techniques to make them, okay. Techniques are not that very important because many of you may never actually work in the fab lab, okay. Very few maybe allowed or maybe trained to do that. By modelling of course CAD is something which everyone does, so be stick to that, so modelling is major in this course majorly involved in this course, okay.

So silicon solar cells are getting into very importance in world over after almost 10 of 20 years. 25 years no one thought of silicon solar cells it has come back heavily now, okay. A lot of money has been pumped in by all governments because suddenly there arise petrol as a problem, okay. You can see how many wars are going on for that, okay. So that is the issue how much corruption on that everything is going with the oil, okay.

The text of this course is founded 3 books, normally do not teach from any book in general but the first book in particular (()) (7:11) reference book on silicon VLSI technology fundamentals practice and modelling, I had only second addition please check it if higher editions are available they will be better. Okay, so this book is available I have not checked it and hopefully available maybe costlier.

So the other book which is not in the print now, so this book is one of the best possible book in 80s or 70s rather. He is the pioneer of VLSI technology or semiconductor technology and his name is Sorab K Gandhi, he is Indian but settled maybe born and brought up in US, I thought so. He is actually from Mumbai, okay. There is another person name I say Chang Sze they have a book on ULSI technology. There are many other books in the library check for them but as I say mostly I will teach from the first book. Mostly now does not mean I will teach from that book, okay but possibly yes most material is available in this first work.

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Course Syllabus

Crystal Growth. Clean rooms. Solid State diffusion modelling and technology. Ion Implantation modelling, technology and damage annealing, characterization of Impurity profiles. Oxidation: Kinetics of Silicon dioxide growth both for thick, thin and ultrathin films. Oxidation technologies in VLSI and ULSI, Characterization of oxide films, High k and low k dielectrics for ULSI. Lithography: Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI; Mask generation. Chemical Vapour Deposition techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films, Epitaxial growth of silicon, modelling and technology. Metal film deposition: Evaporation and sputtering techniques. Failure mechanisms in metal interconnects, Multi-level metallisation schemes. Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques, RTP techniques for annealing, growth and deposition of various films for use in ULSI.

Process integration for NMOS, CMOS ICs.
Introduction to Silicon Solar Cell technologies.

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So we are talking about what kind of things I am going to talk about. I am a dog about crystal growth, diffusion and plans, oxidation, CVDs, PECVDs all kinds of deposition techniques and all models for them, okay. That is most important plant, lithography which is a major crux of all the process going on we will talk about that. We will also look into some failure mechanisms and as I say some silicon solar cell also will be talked.

At the end of the day maybe the important output of this is to show how silicon chip is particular ice is fabricated in a process, there maybe 24 or 30 process steps or mask as they call, total steps would be around 500 when the chip is made but the major step which I say 25 or so may go to 30 to 35 these days and these are something and how can IC is made, okay. Full IC processes in here, all these processes are used to generate an IC. So how an IC is actually made typically we will talk about NMOS and CMOS.

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"Micro to Nano"
A Journey into Integrated Circuit Technology

Lecture No 1

EE669: VLSI TECHNOLOGY
by
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Okay, so we start with something today first lecture is micro to nano, a journey into IC technology.

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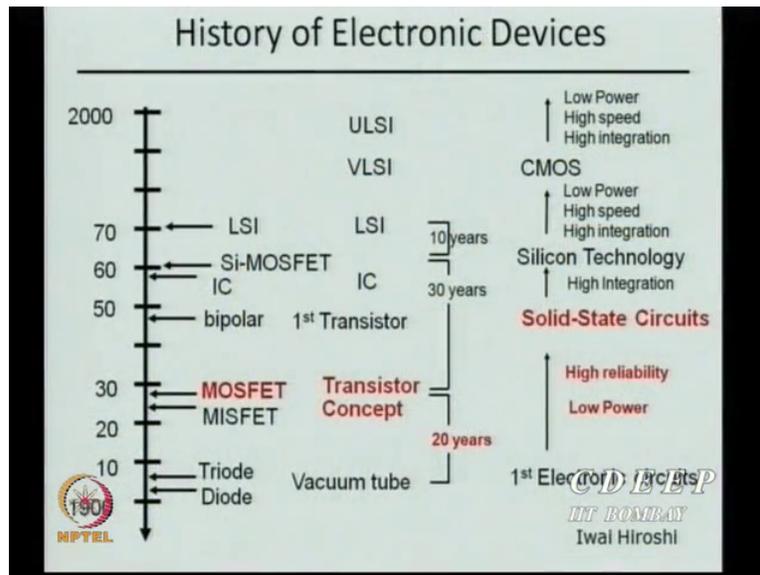


Anything in VLSI or anything electronics for that matter everything in the world these days is related to economics, okay. That is why all these people rule us, you know banks and everyone of you also want to join that because that is where the money is. So actually if you see this is a slightly old slide. (() (9:51) are actually electronic things are in this, there equipment materials, semiconductors, Electronics products and customer demands are all brands of equipments you can see from there, mobile to whatever it is, okay.

Since there are around 30,000 billion dollars business is going on it is very important for us to be a part of it. Just for your own sake I would say hopefully so if some of you may projects in technology hopefully many of you should then there is an...

I hope near Ahmedabad there is a place north of this Palanpur first India's fab will come, okay. There a land has been acquired some work as started this is Hindustan semiconductor manufacturing Centre HSMC like TSMC of Taiwan we have India's now and it is starting with a grope whose ahead is Doctor Viren Verma who was my classmate in Masters. So I am also consulting them, so I am sure maybe 3 years down you will have the first India's fab and we will be working on 32 nanometre process, okay.

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So history if you see from 1900 to 2000 this is an old slide so I did not change about but I can show you hire up later. We started with vacuum tubes diode triode then we went to 30s thought the concept of transistors, concept no transistors. First transistor came in 47 this is essentially from bell lab effort, first MOSFET came in 60 and then we started connecting those components into one.

The most important part of integrate circuit is that all components are made out of the silicon itself or on the vapor itself and that is why it is called the word integration, the metal connection everything, it has no wire there is a connecting line which itself is a connector inside. On the top on the bottom also there are many kinds now. Then if you look at the circuits what is our effort right now?

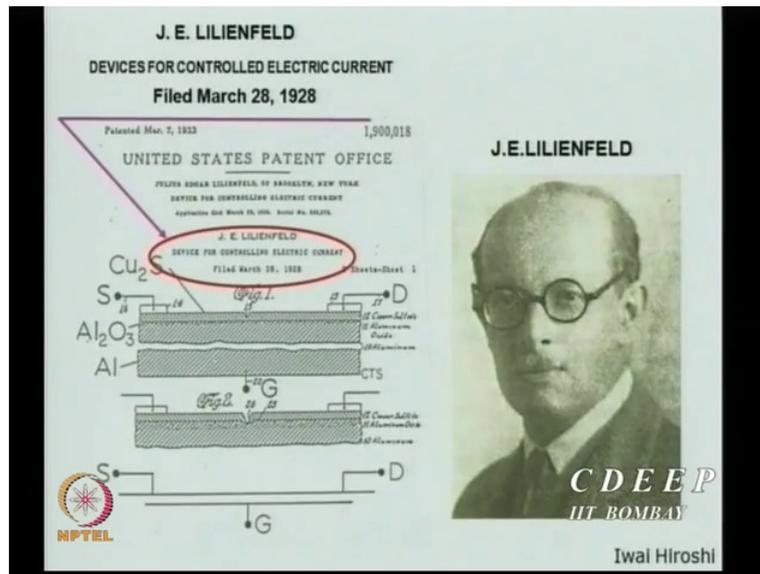
We are looking for first reliability than we are looking for low-power, high-speed, high integration, all kinds of requirement scale and we started putting large number of devices on a chip, typically now we can put 1 billion devices on a single chip, okay. That is the kind of technology we have and sooner we may have 3 to 4 billion devices on chip but I will still give you some sheet this slide later in which getting too many is also not profitable.

First vacuum tube Lee De Forest you can see, I do not know any one of you, maybe your parents also may not have seen but hopefully yes. There used to be a gas tube roughly 2.5 centimetres to

5 centimetres and he used to read the nation as well as transistor equivalents amplification, there are 3 terminals there one here, one here and one here. So one is called the cathode and one is called anode and in between it is called grid.

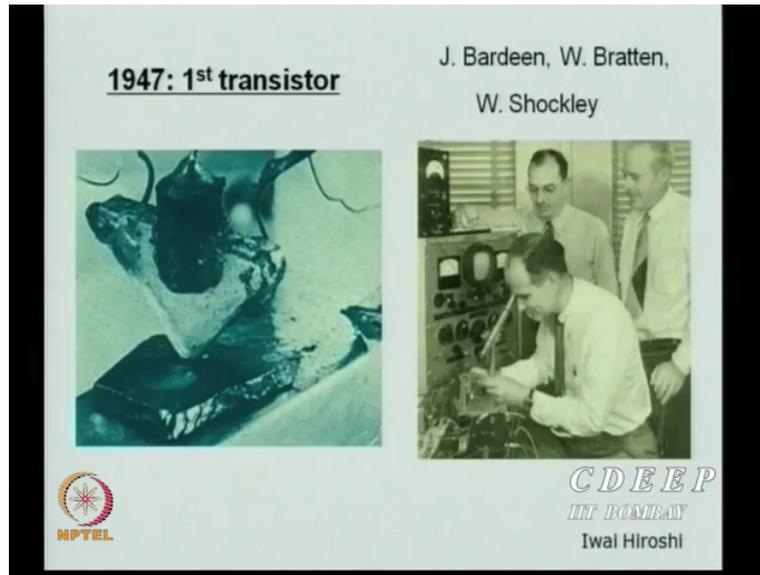
Grid is biased, so that the electron motion from the cathode the anode can be modulated and that is how amplification can be obtained. So this is the first transistor version which appear in 1906 and Lee De forest and Wilson got the Nobel Prize, so it is a very bulky, okay.

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In 28 some Army officer Air Force officer in England actually suggested that you can have a solid-state equivalent device which can control the current from source to (D) (13:58) these names were not given by him this was (S) (14:01) by himself but initially its first paper did not have these names. So what he has? He has a is some aluminium over which he deposited aluminium oxide by oxidation and put 2 contacts which he called source and drain and he figured out that this device can actually connect with in source and drain and get can control the current but he has not made them, okay. He has not made any mass.

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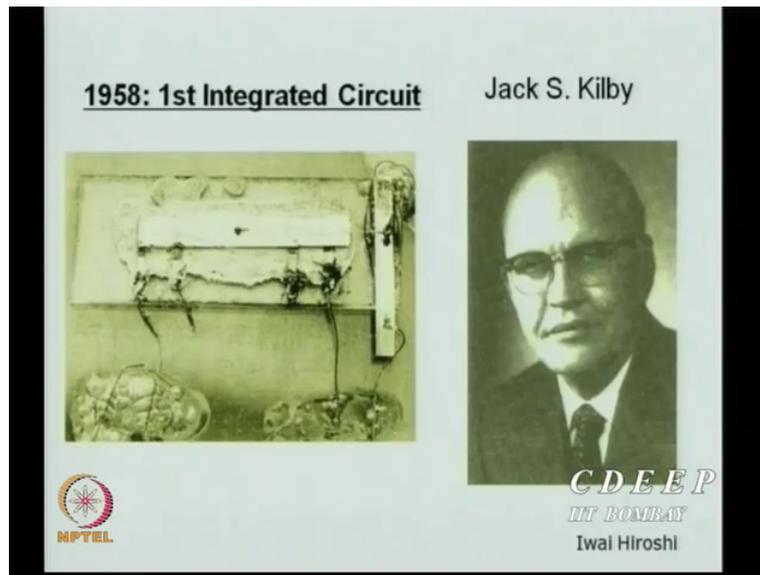
The first transistor which was made was in 1947, the 3 Nobel Prize winners are shown on the right Bardeen, Bratten and Shockley and the first transistor looks as a point contact...

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So there may be better figure, so here you can see how bad it was in those days just to connect things but today the IC looks to be fantastic.

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The first integrated circuit was due to the effort of Jack Kilby at Texas instruments and what he thought that why actually get different comments from separately, so why not use silicon areas itself to create resistor and capacitors and those days we never thought of inductors and here to put some device by Boulder transistors created there itself and connected on silicon chip itself, okay. And that was the first IC.

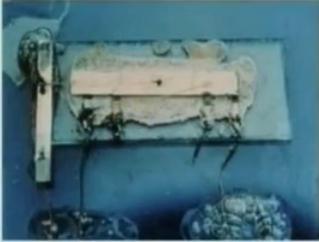
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1958 - Integrated circuit invented

September 12th 1958 Jack Kilby at Texas instrument had built a simple oscillator IC with five integrated components (resistors, capacitors, distributed capacitors and transistors)

In 2000 the importance of the IC was recognized when Kilby shared the Nobel prize in physics with two others. Kilby was cited by the Nobel committee "for his part in the invention of the integrated circuit"



a simple oscillator IC

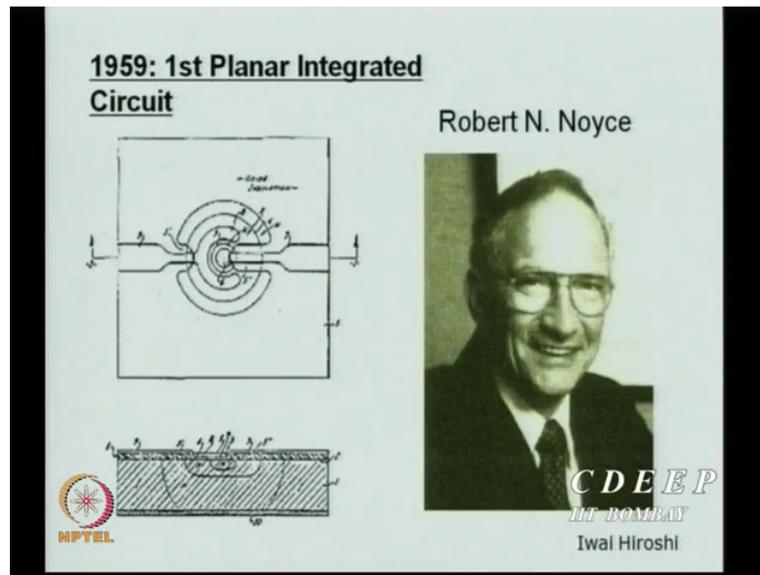
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Just to give an idea in 1958 Jack Kilby at Texas made a symbol oscillator which has 5 IC components, resistor, capacitor, distributed capacitor and transistor and in 2000 the importance of IC was recognized, please look at it. It took 50 years for noble committee to think that this was a great thing, okay. So they avoided him into thousand and which was also shared by him by others. So in 2000 Kilby got his Nobel Prize, the other person who would have got is a next figure I will show was (()) (16:08) but somehow he expired and therefore was not the participant on that. So this is the first IC and just even interesting anecdote Kilby was hired after his graduation by a textile and he had no work to do.

So he was just sitting and reading. So in those days it was not high-pressure in industry, so you were allowed and do something and watch what is going on, training as they called in those days. So used to get bored, so in his off time what to do? So he did this, okay. So think of it even if you are doing idling do something constructive.

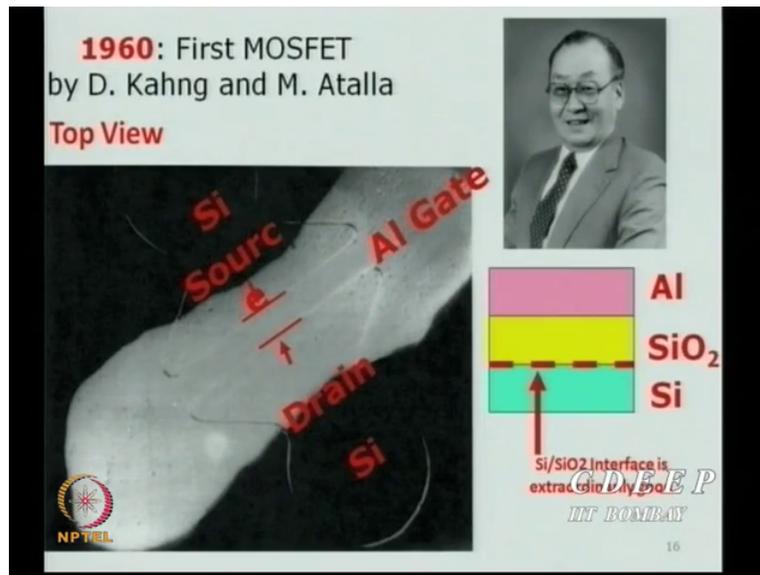
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This is (()) (16:54) he made the, you know earlier transistor (()) (16:57) for example there would be contacts on the bottom side, on the top and it is difficult to put a wire from top to bottom, okay. So only one discrete device could be made, so make an IC how do you connect different devices in some top to bottom, bottom to top connections that is wire will come and that whole integration will be lost.

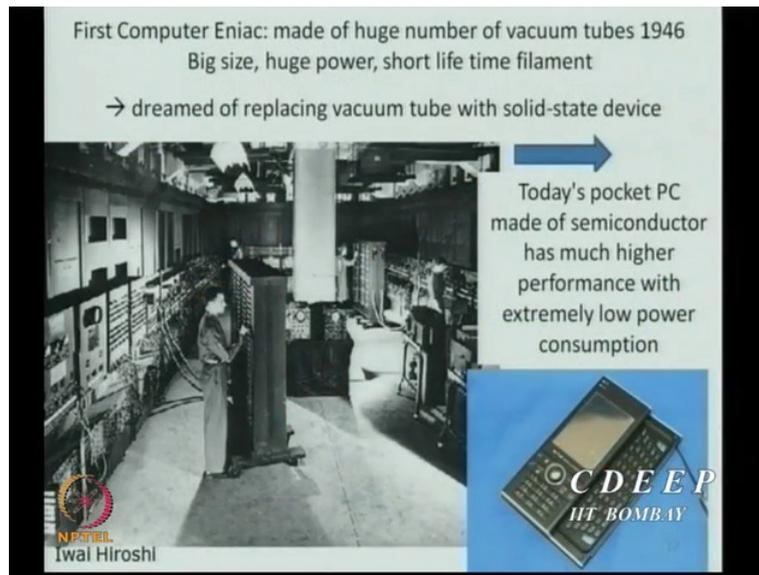
So what he did that he could bring all contacts on one surface? It is called Planetra that was his invention; he said it is a planar technology that was his choice. Now that noise is also very famous for him was one of the founder members among the 3 of the most famous company of world right now in electronics Intel, so he is the founder of Intel, okay.

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In 1960 Bell labs the first MOS transistor was made, 26 people suggested 28, it took almost 32 years before the first device was made. It is a mass capacitor shown here which was created by Kahng and Atalla at Bell labs and one can say semiconductor history is well lab in the history; he was a Korean, okay.

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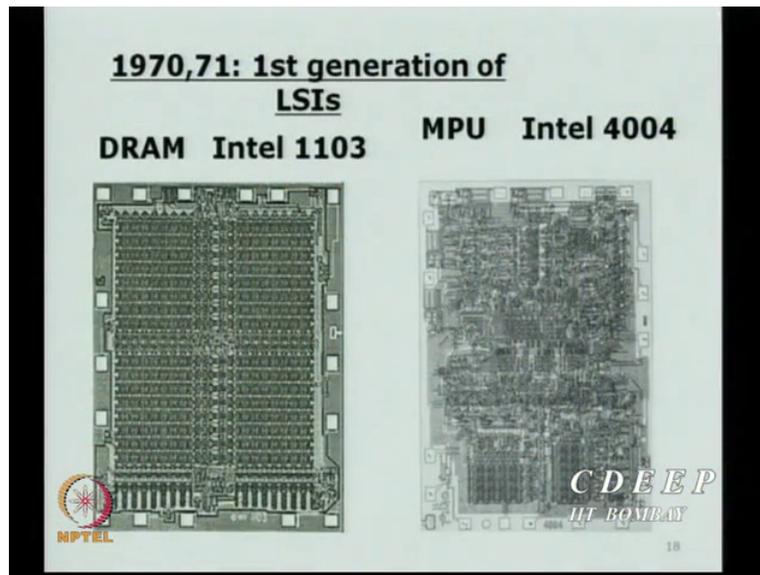


But unfortunately if you see there is no Indian anywhere, okay. We always follow we do not think ahead, okay. So let us start changing this concept sooner. The first vacuum tube-based computer was made in 1946 is called ENIAC it is electronic calculator, okay. And it has which size, huge power, short-lived because the filament which actually generates electron heating it gets used to spoil.

An equivalent vacuum tube probably you know of course these days even that is gone, earlier TV tubes used to be enough, now of course there are solid states but earlier there is a TV tube at least you could say vacuum tube being used. Now most TVs do not have that, there are LCD or LED displays, so they do not even have to use now, so the filament was to heat and it will generate electrons in vacuum and they travel by the voltage or the field and they will be connected and if you moderate them in between, so I can amplify something from the moderating angle.

So this was the first such computer, this is your Pocket PC and that is your computer. Of course it is a smaller part has been shown, it was having around 1 acre of land internally used to create small calculator which does addition, subtraction, multiplication not even division.

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1970-71 first large-scale integration devices came DRAM 4000 K or 4000 bits or 4096 bits this was 1103 from Intel and also there were first microprocessor which was a P channel device, it is 4004 bit microprocessor, this is the first microprocessor made. Of course there is a fight between many other companies than Intel which is still not solved.

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In 2012
Most Recent SD Card



128GB (Byte)
= 128G X 8bit
= 1T(Tera)bit

1T = 10^{12} = 1 Trillion

World Population : 7 Billion
Brain Cell : 10~100 Billion
Stars in Galaxy : 100 Billion

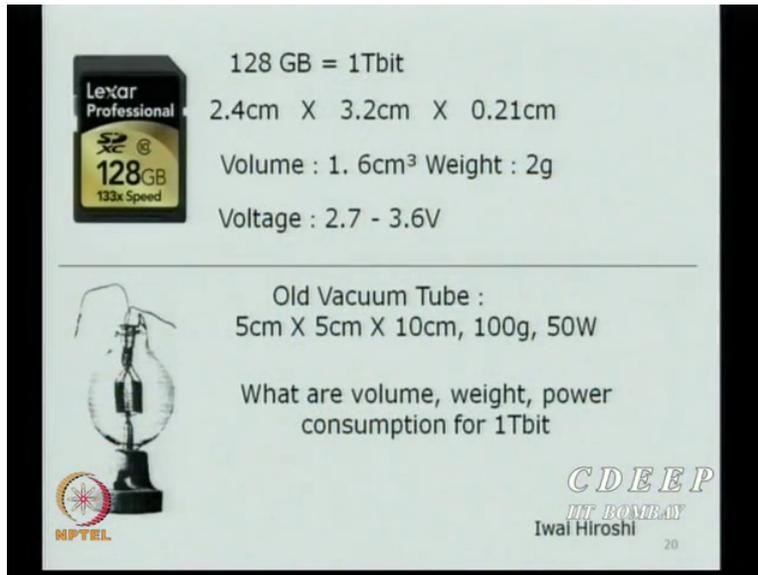
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Just to give an idea the recent SD that is your card which you see on your (()) (20:34) which is typically 128 G bytes, okay. This is the card is available where you put everywhere in every system if it is a byte than 128G into 8 bits which is Tera bits, 10 to power 12 is Tera. Compared world population 7 billion, brain cells 10 to 100 billion this number is varying different people have different brain cells, okay.

Some may have 100, okay. I may have not even 10 now many of them might have burned, okay. Stars in the galaxy 100 million, so we are talking of numbers which is even beyond what one can really perceive and therefore this size is hardly 1 inch by 2.5 inch, thickness may be half a centimetre or even lower, maybe 2 millimetres and you just plug in and you have 128 GB memory available to you.

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128 GB = 1Tbit
2.4cm X 3.2cm X 0.21cm
Volume : 1. 6cm³ Weight : 2g
Voltage : 2.7 - 3.6V

Old Vacuum Tube :
5cm X 5cm X 10cm, 100g, 50W

What are volume, weight, power consumption for 1Tbit

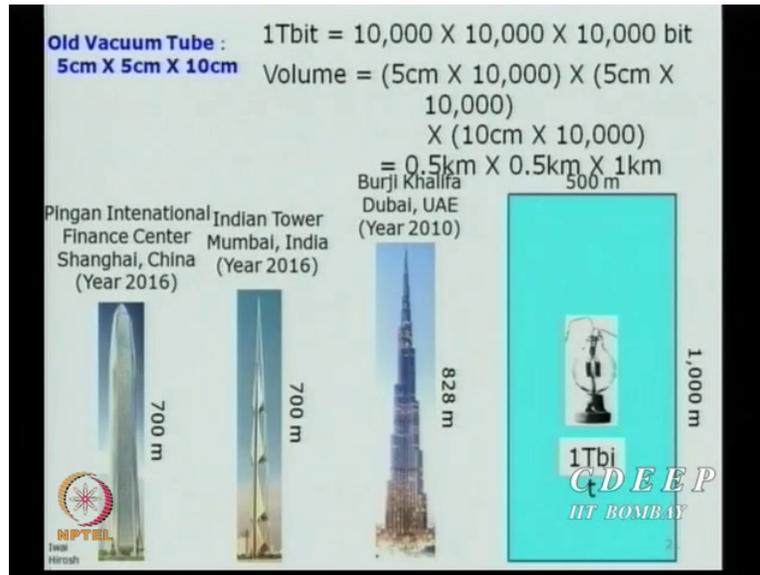
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So the kind of thing technology could do is enormous just take it if I want to make the same, you must have seen many other slide have some borrowed from Iwai Hiroshi. Iwai Hiroshi is a very famous VLSI technology person in Tokyo Institute of technology and (()) (21:59) I am his friend for last 12 years, 15 years or maybe since 98, so maybe 16 years. I visited their lab 8 to 10 times, so many of his PPT that could just (()) (22:12) to show you, okay.

He visits every December, those who wish to visit he has permanent faculty for one month IIT Bombay Department. So let us say you have one this, each of this is 2.4 centimetre by 3.2 by 0.2 1 centimetres. The volume is around 106 centimetre cube CC and 2 grams weight and you typically apply 2.7 to 3.6 volts. Now if you look at old vacuum tube which is 5 centimetres by 5 centimetres let say Equivalent Square if I create and 10 centimetre high, 100 grams weight and it consumes 550 watts of power. Typical voltage you have to apply 300 volts.

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So now equivalently if I create one terabyte something in the vacuum tube what will happen, here is the number 1 terabyte is 10 to the power 12 so I made 444 bits where each of them if I put into vacuum tube given then you can see it as a 500 meters, this 500 meters and this one kilometre down that kind of system I will have to create must make as adequate. The present day other towers of course is the old one which is Shanghai is which is possibly will come in the year 2016 and that is 700 meters.

India is going to build in Mumbai I do not know when, now things are changing it maybe even 7000 meters also, I do not know but the present day which has already been the highest tower in the world is right now 828 meters in Dubai. So look at it even the tower they have made its 800 meters and we are asking 1 kilometre thousand meters, the. So if I have to make one small memory bit this card these many towers this much is also not simple, okay. So the progress what we have done over the years. These are some interesting data which you all should understand how much we are progressed.

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Old Vacuum Tube : 50W

1Tbit = 10^{12} bit

Power = $0.05\text{kW} \times 10^{12} = 50 \text{ TW}$

Nuclear Power Generator 1MkW=1BW

We need 50,000 Nuclear Power Plant for just one 128 GB memory



In Japan they have only 54 Nuclear Power Generator

Last summer Tokyo Electric Power Company (TEPCO) can supply only 55BW.

We need 1000 TEPCO just one 128 GB memory

Imagine how many memories are used in the world!

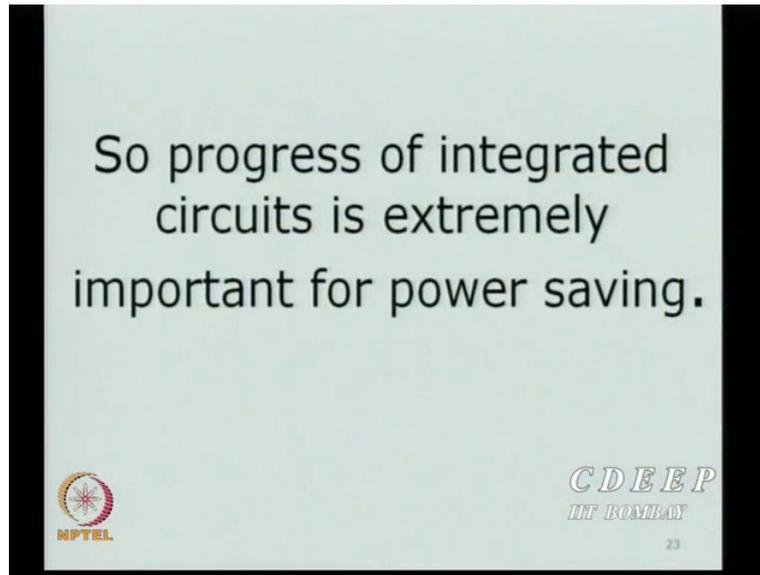
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If you look at the power 1 terabyte 10 to power 12 bits as I said 50 watts of power it consumes in tubes, so it is 50 terawatts. We need 50,000 nuclear power plants for just 128 G B Chip, okay. And example he gave me is in Japan there are only 54 nuclear power plants one of course is down now. Last summer Tokyo Electric Power Co can supply only 55 billion watts, okay.

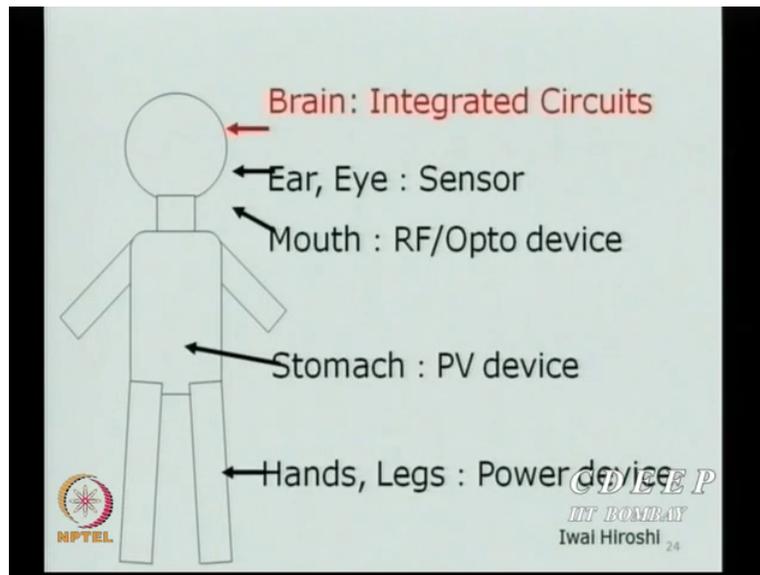
Now you want terawatts for one memory chip. So you need thousands of companies to make 128 G B memory and imagine how many memories are used in cameras and everywhere and electronics, so how much power you would have required just to create a small memory. So think of it, vacuum tubes in those days 1900 it was real great but things where are we now, okay.

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So the progress of integrate circuit is extremely important for power saving if nothing else, okay.
And there were so much nuclear plants you would have to put more just a great one memory.

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If you look at an equivalent in our human ways, you can see your brain is like IC, there are many ICs there which are mostly processors, (()) (25:54) are essentially processors, so there is information which received through sensors, your sensors are ear and eye, your mouth is like an RF slash Opto device actually let's say monitor set, vibrator said and I do we hire frequency and that is how digestion takes place, that is how the vocal cord works, so let say these are the devices which we make and this is what humans are.

Your stomach is something like photovoltaic device huge power is generated out of it, okay. And your hands and legs are like power devices they can move, okay. So already humans are doing whatever is what we are now trying to do and therefore most of the biomedical people keep trying to put equivalents of that. Neurons, this processor, this equivalent, okay. But humans are right now the only thing which so far we cannot imitate all Robo are maybe at least 1 percent of the human capacity, rest of Robo, okay.

Since you are all becoming too smart not just smart everyone wants to do this, okay. And you also demand all kinds of applications, so you need a way high-performance, extremely low-power we do not want to plug-in every now and then, okay. So the most probably the only answer which is relatively low power. Earlier we used to say very 0 power, it is not true, it also consumes hell of a power comparatively.

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Near future smart-society has to treat huge data.

Demand to high-performance and low power CMOS become much more stronger.

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Please take from me that one of the things which will maybe in this course I may not discuss is this current technologies of 30 nanometre Dom maybe even 45 nanometre Dom actually have devices in your cells for mobiles, all mobiles are standby they are not always on but they have to be on because otherwise when the message comes or this it has to be turned on. So (()) (28:07) mode is also there, our on mode is also there and when you can actually shut, shut it off.

So the problem is when the standby mode, okay because standby mode power is consumed even if it is not really working. The problem started in 30 nanometre Dom technology the device is made that the of power is higher than the on power, 66 percent of power, 33 percent on power which means if we just keep your mobile it will leak without you doing actually that is why most of you keep talking 24 hours, okay. So that is some fun part in that.

Semiconductor device market grew 5 times in last 12 years though it is very mature market 2011 to 2025, 300 billion USD was in 2011 and we expect the next 14 years I mean from 11 1500 billion US dollar business, okay. So if that much is the business then you can think how many people will be involved just do this kind of business and therefore the research therefore the effort.

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Cost of chip production

- At 1000 wafers/month (lots of parts!)
 - ~\$600/6 inch 0.25u wafer~\$3.50/cm²
 - Add for packaging ~0.25 cents/pin for QFP (about most expensive)
 - Add for testing \$200/hour for 256 pin mixed signal tester; about 1 second to move sites
- (6 inch wafer ~ 180 cm², 8 inch ~ 310 cm²)

From numbers like these, you can compute production price of your chip

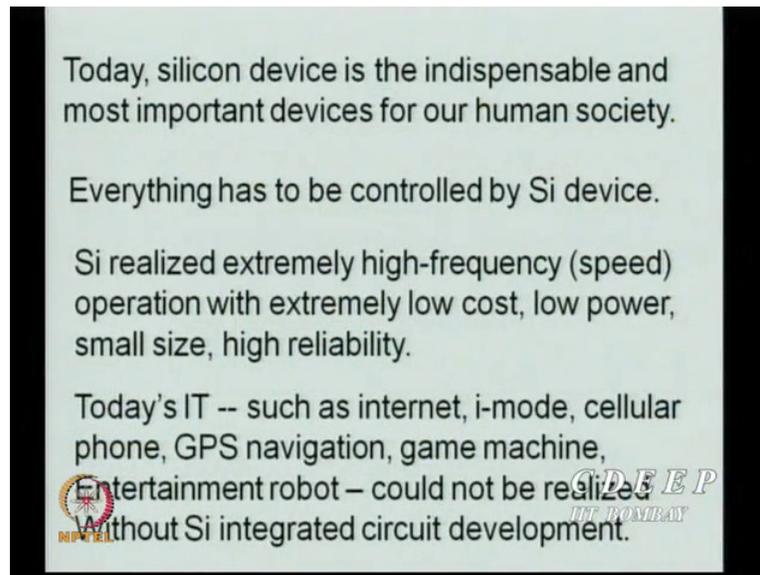
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THE BOMBAY
NPTCL

Thanks to Chuck Neugebauer for prices ca. 2005

How do one calculate cost of the chip, let say we make thousand wafers per month lots of parts in fact. 600 dollar is a 6 inch wafer of course we will show you now it is not 6 inch, it is 12 p to 16 inch, quarter micron thickness, quarter micron so it costs you roughly 3.5 dollar per centimetre square. Add packaging cost of 0.2 5 cents for pin (()) (29:53) or any kinds of package you have, this is very costly part. Package is the costliest part in the chip, okay. Chip is very cheap, okay.

So typically from the numbers you get you find that the cost is calculated, how many chips per wafer you will get? How much per this is their? How much package cost? And then there is your profit. At the end of the day there is a profit otherwise who will sell, okay. So this profit makes industry grow and whenever there is no profit which you see many of you now have good economist than me. I have never gone to the so-called the famous senssex market this year in Mumbai except I used to see when I was in TIF for the tower. I have no money to really invest, so I could not go there, okay. So I figured out that those people are deciding that what we should do which is very funny but that is how the money matters, okay.

(Refer Slide Time: 30:58)



Today, silicon device is the indispensable and most important devices for our human society.

Everything has to be controlled by Si device.

Si realized extremely high-frequency (speed) operation with extremely low cost, low power, small size, high reliability.

Today's IT -- such as internet, i-mode, cellular phone, GPS navigation, game machine, Entertainment robot – could not be realized Without Si integrated circuit development.

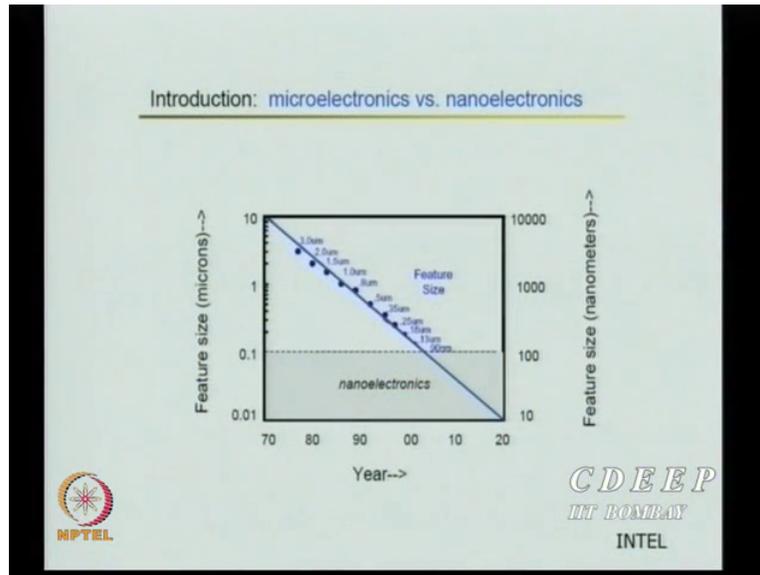
GDEP
IIT BOMBAY

Today the silicon device is indispensable, most important devices for our human society. Everything has to be controlled by silicon. Silicon realized extremely high frequency, high-speed operation with extremely low cost, low power, small size, reliable. Today's IT industry or today's IT products if you see such as Internet, i-mode, cellular, GPS, game machine, entertainment Robo. They could not have been realized is would not have been silicon IC itself.

Along the entertainment it is really interesting that the major market for an interior circuit is in this game machine. Luckily in India, so far it has not been profitable there are these PlayStation's across most of the cities in the world. In Tokyo at least there are thousand I know where I have been, there are 4 to 5 on every street and I do not know what whole night TA TA TA they keep doing and enjoy, fine. They have money so they enjoy, okay. So are you doing these days it seems?

So what is that is driving us last 100 years. If you see we started a vacuum tube in 900 let say up to 2000 it went from 10 centimetre kind of size to 100 nanometres below now. So typically hundred years we have 1 million times reduction in sizes which was remarkable, okay.

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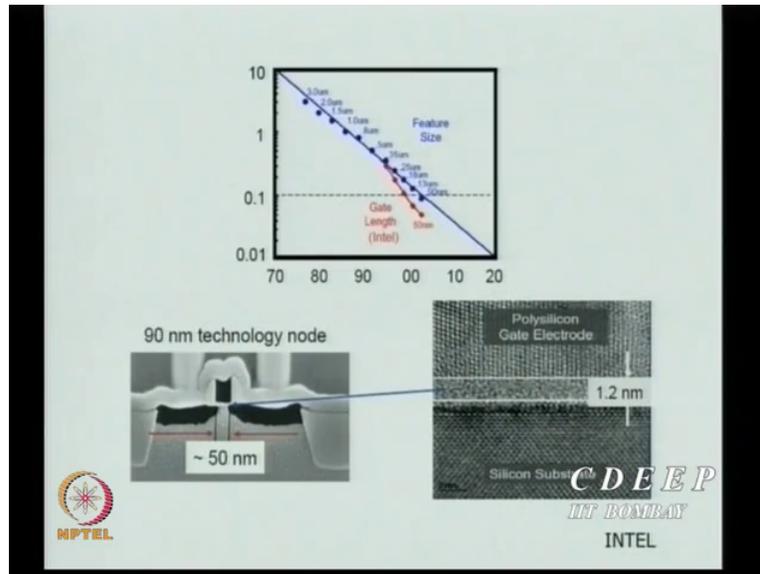
Suddenly into thousand people started for getting the word micro and they invented the word nano. Now this word micro to nano is not very fair and this is the gap which I always show and prove my point. The left side this side is the microns and this side is nano. So if you see up to 0.1 micron which is 100 nanometres we then started from few microns, 10 micron structures down to 90 nanometres by 2000 and below 90 nanometre we say it is nano. Only one of the dimensions was less than 100 nanometres and we suddenly jumped into because it looked the all politicians, bureaucrats they have fancy for new words.

So they only pay you project wise, if I say I will make the microchip they will say no money I want nanochip, how much? If I say I am going to teach 150 students that salary is enough what else you want? If I say I am going to teach 10,000 colleges, 5000 percent from here, how much many? No problem there is huge money with us. So there is some number game going on, okay. So is a nano CMOS.

Of course nineties not bad and we have now reached this state we should latter is around 60 nanometre we are already working at but the game is nano word started when we crossed 100 nanometres and only channel length was less than nanometres. So we suddenly became new name, new money, okay. That is how CN appeared, if I would say Centre for microelectronics no one would have paid. Now I know it is something there, pay the money, 200 crores we got I

mean you fool them well, okay. Not that we are not doing anything I mean this money they would not have given the few would have not put the word nano, okay.

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So luckily for us this nano this is some graph which I initially showed you, this direction below nano it somehow not going in that slope, particularly the gate length and the gate length is not scaling down, okay, in the same proportion and therefore some respite is there for a technology manner. You scale exactly same way then technology has a tough time to match, okay.

However for example a 90 nanometre node its actual gate length is the nanometres and if you are (()) (35:18) it sicknesses 1.2 nanometres 12 angstroms, okay. Now this scaling down is very important, why are we scaling? We went from large microns 10 microns to 5 microns, my first chip of India along with (()) (35:36) of our other colleagues, few of them are here Professor Dinesh Sharma was my colleague then afterwards just resign and left he was my colleague and percept into who actually manages our lab is also from (()) (35:48) and few more other and many (()) (35:51) faculty after retirement joined here, that is me, okay.

So because of us we were first to make first IC in 1979-80's time there I must honestly say did not work fully but it was made partly it was work it was shown to Indira Gandhi, so all of us had kept behind only my professor was ahead, okay who probably did not know how we made it,

okay that is how professors are, okay. Why professors actually do this? Because if you know it you will do it, if you do not know you will teach it, is not it? That is the way it is.

However I must tell you that first 25 years I actually worked in the lab, so I am not one of those faculties who are never been to lab I worked many devices in (()) (36:41) and all photo diode I have made many many devices in my career Micro devices, so I am not saying that but generally this is what most people believe (TEACHER KO KYA HAI EK GHANTA PADAYA MAJA HI MAJA) it is not like that.

(Refer Slide Time: 36:59)

1900 **"Electronics" started.**
Device: **Vacuum tube**
Device feature size: **Several cm**
Major Appl.: Amplifier (Radio, TV, Wireless etc.)
→ **Technology Revolution**

1970 **"Micro-Electronics" started.**
Device: **Si MOS integrated circuits**
Device feature size: **10 μm**
Major Appl.: Digital (Computer, PC, etc.)
→ **Technology Revolution**

So in 1900 Electronics started applications amplifier, radio, TV, wireless. In 1970 microelectronics started, silicon IC's came, device feature where 10 microns or lower slightly, applications where still digital, compute, PCs it was a technology revolution then.

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2000 **"Nano-Electronics" started.**

Device: **Still, Si CMOS integrated circuits**

Device feature size: **100 nm**

Major Appl.: Digital (μ -processor, cell phone, etc.)

→Technology Revolution??

Maybe, **just evolution and innovation!**

**But great evolution or innovations!
and so many innovations!**



And in 2000 nano electronics started, device is still, silicon CMOS IC, features are less than 100 nanometres, major applications are still microprocessors, cell phones and there is a technology revolution maybe just evolution and innovation but great evolution or innovations and so many innovations. If you think keep going this you can understand where we probably made each, okay.

(Refer Slide Time: 37:55)

Now, 2014 "**Nano-Electronics**" continued.
Device: **Still, Si CMOS integrated circuits**
Device feature size: **around 10 nm**
Major Appl.: Still Digital (μ -processor, cell phone,
etc.)

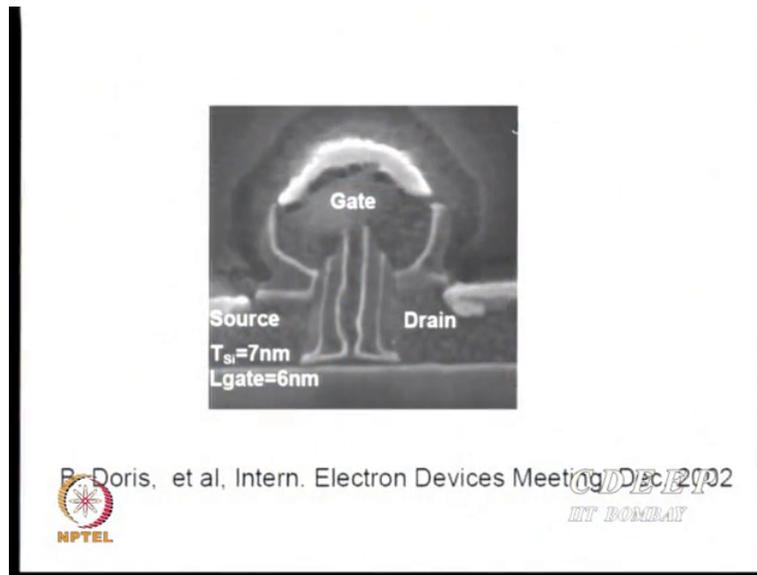
Still evolution and innovation.



2014 nano electronics continued still silicon CMOS around the nanometres still digital, okay, still evolution and innovation is continued. So think of it since I may not survive 2025 I hope so I mean I wish I do not have to survive beyond that itself I mean even now I am enough old but I can at least say 2025 silicon CMOS will not go, okay. Beyond that I may not, so I may say maybe if it happens in 2050 also, so it is okay.

I may not be answerable but 2025 I can assure you silicon technology cannot be defeated by the other material technologies whatever they may say, whatever they may claim for taking money, okay. Otherwise silicon ICs cannot be replaced, okay take from me, okay.

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This was in 2002, 7 nanometre gate first transistor were made though of course it was not an IC it was an isolated device. So even as early as 2000, 12 years ago the first device with 7 nanometre was made, okay. So think of it technology going from lab to a actual fab House takes 10 years even now 7 we have not reached, okay. Research is a part of the game ikeep doing, keep doing someday someone will pick it.

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Last few slides, all of us are looking for TERA instructions per second, mega floors and this alright PETA, we are looking for TERA more than TERA in fact. So we are looking for processors which can give 1 tips instruction by 2012 actually we have not reached so far we may reach, okay soon. We started at 80-84 to 4004 I did not write but 80-85, 80-86, 286, 386 Pentium (()) (39:53) I think many of those name appeared but still we have to reach normal case rather than in (()) (40:00) is okay quad may do but quad has another problem or at a time working synchronizing is very difficult, sharing memories is also difficult, okay.

Though it is the major way people are increasing the speed, so our number of instructions per second but by a single microprocessor with ability of one Tera instructions per second is still to be achieved though we thought 2012 it will but 2014 it has not reached.

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Technology Scaling

Dimensions scale down by 30%	Doubles transistor density
Oxide thickness scales down	Faster transistor, higher performance
V _{dd} & V _t scaling	Lower active power

Technology has scaled well, will it in the future? *CDEEP*
IIT BOMBAY

So what is the gain in this technology in and why we are learning over the year's new technologies? Because even if this is a mass device I trust many of you are aware now. In 1980s people did not know a mass transistor. The mass transistor theory is to be 2 to 3 pages in Millman Halkias in those days that was microelectronics, or knows why they call it microelectronics?

And whenever we will interview for his MTEch entrance he will exactly draw the figure which is vertical mass device which never existed actually, our silicon planar it will go down but here they show you a source drain gate because that is the figure given in the Millman Halkias then he will say carriers are generated because the minority carriers. I keep telling minority carriers so small how much current?

No know that is what Millman gives, Millman was our circuit man he did not know anything of physics, so he keeps telling nonsense and everyone here and tell me the same thing, so I have to keep telling them this is wrong sir please listen from me. So the mass device was so much odd for most of the engineering institutions that they came only with bipolar. So the question was asked that why bipolar was left and why suddenly MOS came in?

2 reasons one can see, one is bipolar require larger power supply voltages compared to MOS and they were not scalable. Like MOS as I said we keep scaling down by some ratio performance

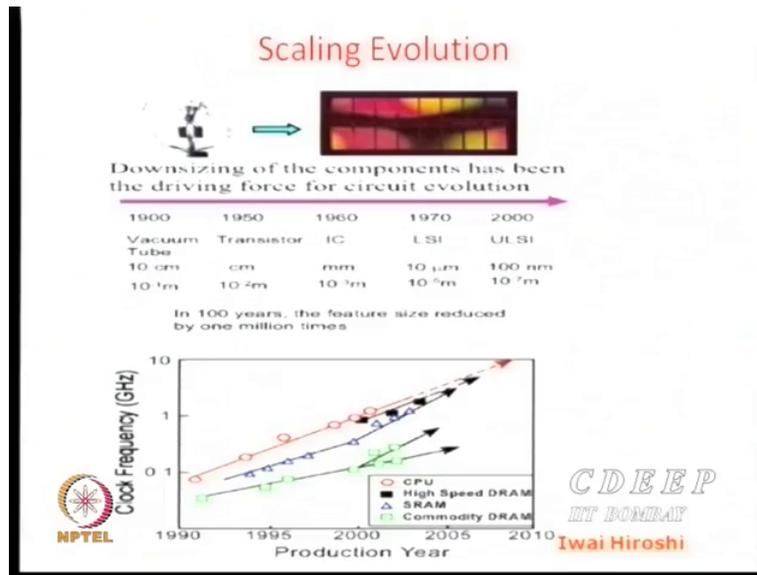
still can be achieved, better performance is achieved but the bipolar scaling was just not possible base width could not be made 0. So you cannot scale base with too much, okay.

So bipolar technology being costlier, more power consuming, suddenly could not match the number of devices required on a chip would be smaller in bipolar compared to MOS so in every sphere it was not able to and costly. So then they say why continue but 2000 again we are still continuing with some bipolar processes and simply because they are very high-speed but they are not in silicon, okay. They are working on 3 to 5 materials where the mobility is the important part and there bipolar circuits are coming back at least part of the bipolar and part of the MOS is can be together called BiCMOS but otherwise bipolar is out for all practical purpose even the Op Amp 741 initially we started with bipolar Op Amp 741 but nowadays you cannot get one all MOS and MOS are CMOS by Op Amp (()) (43:16). So whole and everyone looking for money and everyone looking for better performance have shifted to MOS.

So here is a MOS device I hope many of you know, this is the silicon, this is source, this is one diffused area, this is drained, this is a gate and then between gate and substrate the thin insulator layer which earlier used to be silicon dioxide and even now many devices are silicon dioxide. So if this is effective as the length between source and drain, W is the width of the gate or transistor.

So if we just reduce the dimension by 30 percent transistor density doubles, if the thickness of oxide is scaled down we can have faster because electrons taking time to go from source to drain will be reduced, speed will be higher, better performance and if I scale power supply and threshold I may get low-power so the whole game now is to reduce everything scale down everything, so that you have better performance and much more density of the devices on a chip.

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So what is in future? This is the same the (()) (44:44) only you can see the figure, the graph figure of this frequency versus year. We are expecting around 2010 a CPA should reach 10 gigahertz or even earlier but we have not, okay. The problem is that that we cannot do probably we can hit it some way but cost would be so high that is not worth, okay. Firstly how many of you really want to use a processor which is more than say 6 gigahertz, mostly you use 3.4 to 4.2 gigahertz.

So really fast processors are required only for those gaming interested person who wants to kill the person on the screen before he still starts, okay. So only for videogames probably you need much faster processors, okay. Or if you are doing a large amount of arithmetic or large amount of numerical crunching maybe a new decimal computer which should be we high-speed, okay. One looks for Tera if possible.

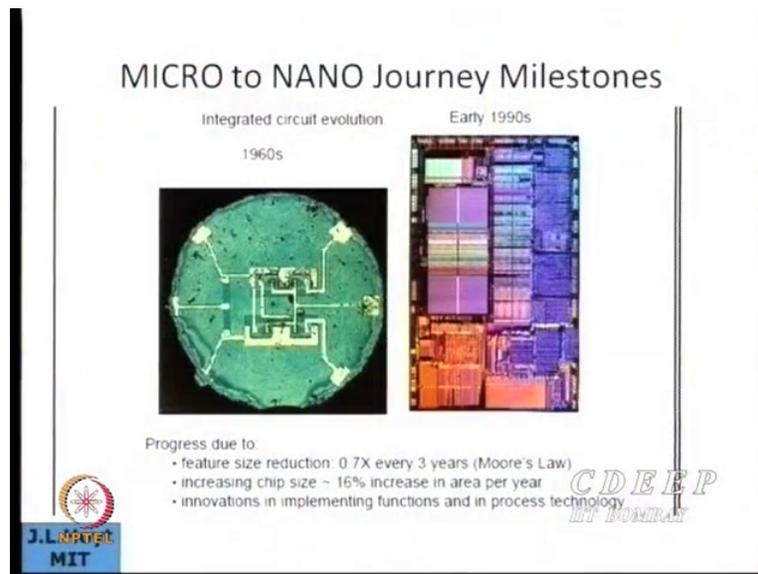
There also what we are doing is what we have done is we have paralleling, merging then one of them fails, all of them fails, so all that so-called supercomputers in India which you listen you must congratulates them for putting so many parallel series combination and every now and then failing that they do not tell because anything in series in one phase the series chain goes, okay.

In parallel it one of them drives more current the other fails, okay. So paralleling is not the best solution, okay. That is why Intel is still not going beyond core processor pad that is it because

paralleling has its own problems, okay. Though it is one of the better solution to increase speed. So I do not think even in 2025 we may cross 10 gigahertz though we believe we should be able to.

At least in silicon it is not possible, other materials maybe we do not know something which is not known I should not say but I think there will not be enough use to go for that. All the industries work on how many people by how much, okay.

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So this is the journey first IC has 4 transistors few resistors and in early nineties this was the Intel first processor chip which was Pentium 1, okay. So what is a law which is actually allowing scaling and I will show you the graph little later. What he said a famous person who was the founder member of Intel? By the way Noyce (()) (47:29) and Gordon Moore and others they are all members of Shockley lab earlier and Shockley started his own company leaving Bell labs. All of them came and started in California.

What happened there, Shockley's nature was very bad and at least that is what reported I have not met him, so I do not know. Gordon Moore I have met, so I can tell you something but others I do not know, so because that then these people were so annoyed, so they joined a company called Fairchild. Fairchild was a camera company, okay. So camera company has some chips

requirement, so these people actually joined Fairchild and in clandestine way or otherwise they actually started working for logic chips, okay.

Designing, how to fab and all? And when they were (()) (48:23) some blueprint they separated and started Intel, some people from Intel also did the same thing and they started AMD, unfortunately AMD could not stand great competition with...

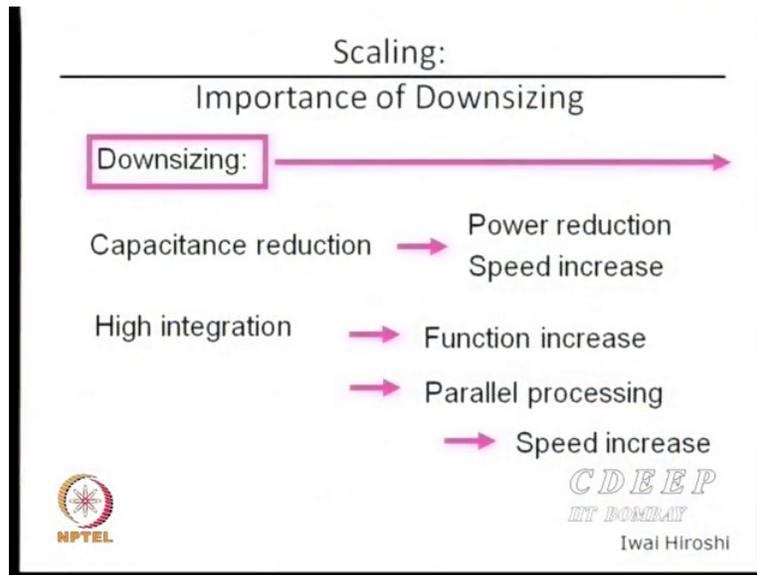
It was also another company which started equally well was Motorola, which I do know for God sake why it has happened? It lost market everywhere wherever it entered; the last one is mobile Google purchased Moto market and then sold it out to Lenovo, okay. So I do not know there is some problem with the word Moto, I have a Moto right now. My son gave me this, so I am still struggling with this smart word there, okay.

So this problem which we started is that number of devices to be put in larger number created a lot of other problems, okay, how to connect them? So what Moore said every few scaled-down, earlier of course he said every year but now every 3 years he changed recently is called Moore's third law, 0.7 times, you scale dimensions, so 0.7 into 0.7 is 49, 0.4 9 which is half. So obviously if your area goes half, so the component density will double, okay.

Half, half, double that was the law he gave, actually it was an exponentially law he took it to binary and declared that as his law Moore's law. It was done way back in sixties and surprisingly in 2014 they are still talking about Moore's law and all the technology people designers keep watching that Moore's law, oh! I must reach the, okay. As if that is sacrosanct, that is what Gospel but that is what the Moore is great visionary, that time in 1964-1965 the technology was not even MOS it was a bipolar process.

MOS devices just started coming, Intel started making first logic on PMOS and then suddenly this law came, so great man I must say accordingly. So what is the advantage of scaling? You reduce the capacitance, so you reduce power and increase speed, why speed?

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Because of the capacitance goes down, charging a capacitor if it is smaller the current require is CDV by DT . So if C is smaller obviously charging current is smaller. Time taken will be for a larger current higher speeds. So that is how first advantage we see can speed up just reducing size. To integrate then many functions can be integrated, so many not just processors you can put everything on chip, okay.

So that is number of functions you have arithmetic, we have shift resistors, we have all kinds of circuit blocks which you can put on a single chip. So lot of functions could be created and of course as I said further processing is possible 2 at a time all 3 at time therefore improve the speed. So this is all possible simply because I reducing the damage and of the device which is called scaling law which is Moore's law, okay.

You scale, okay. However that scale as I showed you is not going straight, now it is slightly bent down, so now what he said every 3 years it will increase, a new law, okay. Then someday he will say 5 years.

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Demand for future VLSI:

Much higher performance
Much lower power consumption

Thus, downsizing of Si devices is
the most important and critical issue.



Iwai Hiroshi

See what is the demand from future VLSI much higher performance, much lower power consumption and therefore downsizing or reducing silicon devices is the most important and very critical issue for all technology and designer that is why every year we have to change technology because the demand will come from videogame site for example I want this then everyone will work for 2 years, you know to somehow give them any reason other than the say no this is not enough. So we are again going to work for it that is all we are chasing money to some extent and improving. So this will continue 2025 beyond I do not know.

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Prediction of Scaling limit		
Vacuum tube era : even μm size could not be imagined		
Since Si IC started		
Period	Expected limit(size)	Cause
Late 1970's	1 μm :	SCE
Early 1980's	0.5 μm :	S/D resistance
Early 1980's	0.25 μm :	Direct-tunneling of gate SiO_2
Late 1980's	0.1 μm :	'0.1 μm brick wall' (various)
Today	50nm:	'Red brick wall' (various)
Today	10nm:	Fundamental?

There are limits coming, there are effects called Chart channel effect, there are resistance effect, direct these are failure mechanisms, okay on the right cause which we said everyone is saying in 1987 or 1978 book by Mead and Conway the first VLSI design book in the world. Mead is a very famous. So Conway and Mead said that you do not need no technology to design a chip because he himself was a technology man earlier but he said so these are called design rules.

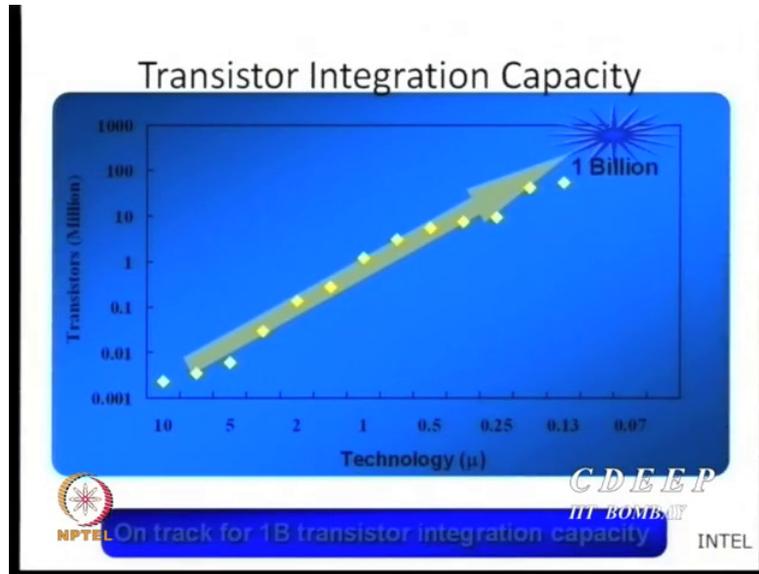
Technology will give constraints so these constraints actually are essentially where up to you can go, so he said by 1987 no more progress will be done, 2014 still progress has been done, so sometimes no one is like Moore, Moore always said it will however buy his physics is said no it cannot but it did, so what has happened? Why Conway for that fundamental limits will be crossed and why?

Because you know we all understand physics but silicon does not it behaves the way it wants, that is way, so give me silicon, okay. So by today we are working on 10 nanometres, 7 nanometres maybe someday. So wherever there is something not possible there is an association which I will show you.

Okay last few pounds before I come back it is called ITRS that is the industrial technological roadmap these people who made some 100 to 500 papers in different areas join and predict what

is next every next year. So there ITI has also said that there is something you cannot do, so they put what we call red brick in that map, you cannot cross this but Indians are smart, so are worldwide, so they made a small hole and got in, okay. No one jumped because redbrick is bigger inside. So you cannot cross thermionically then end it okay. So nowhere tunnel devices appeared, okay.

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So earlier as I said we are expecting 1 million transistor is already on the way, this is the Moore's law I did not put its face but it's okay, this is also old law but still, so one can see if you see here and if you see the number of transistor per die, the topmost is essentially memory, so yes we have already reached as far memories of 256 megabytes (()) (55:29), (()) (55:30) of course we are gone to 64 to 128 to 256 Gbits.

Processors we have Itanium actually is increasing on this, yes there are billion transistor on chip now, so we are still following Moore's Law, okay to great exchange, only thing in slope which changes means number of years required to reach the higher values engaging but that is okay it is not saturated, the whole game is Moore's Law is still valid it is not saturated and that is something this person has to be this.

So at that time he said from one year we change it to 18 months in 2003 and 2012 he said every 3 years it will be doubled all that he modified it, Moore's third law as they say. So you can see

typically this is an exponential law which was being followed and he say double 2.7 is a bad number, so he made it double.

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The slide is titled "Limits of Moore's Law?". It contains the following text:

- Growth expected until 30 nm gate length (currently: 180 nm)
 - size halved every 18 mos. - reached in
 $2001 + 1.5 \log_2((180/30)^2) = 2009$
 - what then?
- Paradigm shift needed in fabrication process

At the bottom left is the NPTEL logo, and at the bottom right is the CDDEEP IIT Bombay logo.

So let say we were at 1 nanometre and we wanted to reach 30 nanometres, size Halved every 18 months let's say in those days. So Moore has given a formula which is interesting whichever year you are in whatever technology, okay. So it is 2001, 1.5 is 18 by 12, so it is one, so you adjust that actual numbers there multiplied by the technology in that year divided by the technology you want to reach and you will get some number of years that is the Moore's law which no book will give this is I got from Moore, so I can tell you.

It is the year, whichever year your technology is today let say 2013 or 14 and let say 3 years he say so 36 divided by 12, so it will be $3 \log_2$, you are working on let say 60 nanometre I want to reach 6 or 5 put it there find which year roughly this technology will be reached, this is Moore's law, okay. Of course question arises what then? God knows.

What power that means paradigms shift essentially that means we will have to change ever thinking, right now what we are thinking is what Moore says, we think, okay. Moore says this year you have to reach here, running, running and then we think we are just there that is what we are trying but let us not think Moore, think something different none of us, none of the people have thought so far.

Yes there are quantum and everything I will show you tomorrow in after tomorrow many devices which are come which are good in lab good on cap Tools but no one is making any chip on that, cost and reliability is very poor, so unless you really go to silicon equivalent CMOS no one is going to put money. A typical fab lab for a one technology node, let say Intel has just put 11 nanometre technology node and invested 8 billion dollars, okay.

The Hindustan semiconductor, our company we have invested 6 billion dollars, remains I have not paid any money I do not have that money, my classmate has he is a venture capital himself, so he has lot of money and he has borrowed lot of money including 2 billion dollars from government of India. So that is the thing which would leave. So Moore is not the end of it but as I say silicon does not understand anything it may still do something wonders.

Now question arises many people ask us over the years, initially wafers are 1 inch wafers silicon wafers then we went for 3 inch then we went for 6 inch then we went for 8 inch then to 12 inch now we are going for 16 inch, so why not we started 16 inch itself?

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Technological Background of the Moore's Law

- To accommodate this change, the size of the silicon wafers on which the integrated circuits are fabricated have also increased by a very significant factor – from the 2 and 3 inches diameter wafers to the 8 inches (200 mm) and 12 inches (300 mm) diameter wafers.
- Soon 16 Inch wafers are going to be introduced.
- The latest catch phrase in semiconductor technology (as well as in other material science) is nanotechnology – usually referring to GaAs devices based on quantum mechanical phenomena
- These devices have feature size (such as film thickness, line width etc) measured in nanometres or 10^{-9} metres

Firstly the growth condition that is what the first part of crystal growth, what are the problems to create larger size wafers and what is a problem there? So now of course we are looking for 16 inch wafers.

The latest technology catchphrase is talk of nanotechnology but if you ask me nanotechnology existed way back thousands years, molecules, atoms are of nano sizes chemist people are always nanotechnologies, so why are we now calling ourselves nano they existed alchemy was known some 1000, 2000, 5000 years. So anyone who works on molecules or atoms probably is a nanotechnology we only converted to silicon what could be done and therefore we became greater we thought no one things otherwise we only.

So now everyone wants to work on nanotechnology and then suddenly found silicon may not be the better material, so look for 3 to 5 compound materials group for quantum mechanical phenomenas, (()) (60:34) some charge phenomena's, (()) (60:37) automata many other interesting physics-based devices comes spin transistors all these are good, fantastic okay but I think so it will work for next 20 years not for at least 25, I do not know I had...

The future size of the order of 10 to power minus 9 meters nano, so I will have them who are working below this our nanotechnologist.

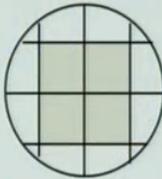
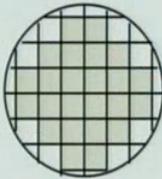
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Recurring Costs

Variable Cost = (Cost of (Die + Die test + packaging)) / Final Test Yield

Cost of Die = (Cost of wafer) / (Dies per wafer x Die Yield)

$$\text{Die per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{Die area}} = \frac{\pi \times \text{wafer diameter}}{1.414 \times \text{Die area}}$$




Die yield = $[1 + (\text{defects per unit area} \times \text{Die area})/\alpha]^{-\alpha}$

Just to give your cost, you know how if you increase the die, die is the smaller chip area in a wafer 6 inch, 12 inch whatever size you have some rectangle, sum squares which forms one die which is the circuit, okay. So for example 2 shown here and this is your larger die size the other

one is a smaller die size because questions were asked that why not be started larger die size day one, okay.

So here your answer for this, so let us say if you say this is larger and this is smaller, so there are different costs involved and as I said industry only works on cost and nothing else. If you say it is very good they will say okay then keep it with you what is good as money. So if I can fetch money more than all technologies are good. So do not say that 90 nanometres is worst, yes for many applications 90 nanometres technology is fantastic it is doing all that job what people are asking, so why invest money just because you want?

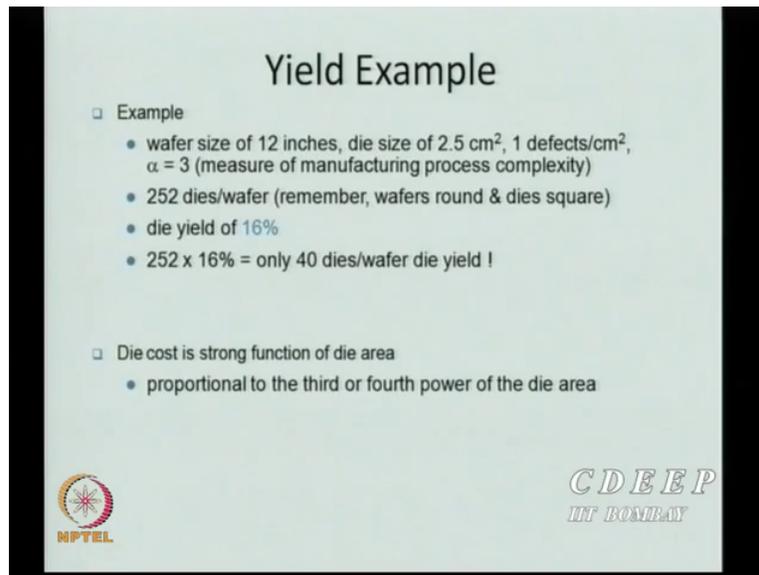
No industry will only do as much as what is demanded. So the cost of, it is called variable cost depend on the die size, die test, packaging and the yield. Yield means how many good chips out of 1 wafer it is called die yield, total yield and then each wafer has a die, die itself may not work, so it is called die yield some part may work. So the cost of die can be given by cost of wafer divided by dies per wafer into die yield.

Now what is the definition? Die per wafer can be define from its area and parameters, okay and this is a formula which I got from somewhere by wafer diameter by 2 square upon die area minus pie wafer diameter into root 2 die area, this is parameter based and this is area based. Now I can calculate die per wafer, I know how many good dies are available, so I know dies per wafer into die yield and I know how much is the cost of a wafer, okay.

So I know what is the cost of each die and if I know my cost of each die and if I want to calculate die yield, we have another formula which says it is one plus defects per unit area into die area. Now these defects are the one which is material defects which may be created during fab unknowingly by knowingly also they are there even if we know I cannot remove them or during actual chip operation also if it can start, okay.

So based on this formula 1 plus defects per unit area into die area, so Alpha is technology parameter will give some interesting numbers which I calculated yesterday.

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Yield Example

- Example
 - wafer size of 12 inches, die size of 2.5 cm², 1 defects/cm², $\alpha = 3$ (measure of manufacturing process complexity)
 - 252 dies/wafer (remember, wafers round & dies square)
 - die yield of 16%
 - 252 x 16% = only 40 dies/wafer die yield !
- Die cost is strong function of die area
 - proportional to the third or fourth power of the die area

So wafer size let's say of 12 inch, let's say each die is 2.5 centimetre square that is 1.2 by 1.2 centimetres. Let say each centimetre square has one defect which is many times larger but these days technology is improving. 252 dies per wafer we can get from the...

Please remember wafer is circular, die is square so obviously edge chips are not possible. So typically 252 dies per wafer one can get for 12 inch wafer if you are die size is 2.5 centimetre square. Let say you have die yield of 16 percent due to defects which is what the worry is, okay. So only 40 dies per wafer out of 250 are available, so you can think of it if any industry has to work if it says that only one sixth of the chips are I mean devices are dies are working then it is too costly for them, okay.

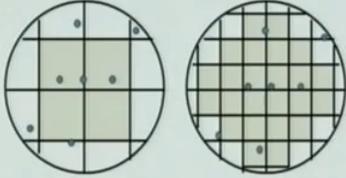
So the cost is something now related to defects, how many defects in process you get? That is why you need better process. So one can see from here if I have larger real then your cost goes down, larger yield, okay. If your die yield is higher obviously you can see your variable cost would be smaller. So the game in the actual processing is to reduce defects, okay.

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Recurring Costs

Variable Cost = (Cost of (Die + Die test + packaging)) / Final Test Yield

Cost of Die = (Cost of wafer) / (Dies per wafer x Die Yield)

$$\text{Die per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{Die area}} = \frac{\pi \times \text{wafer diameter}}{1.414 \times \text{Die area}}$$


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Die yield = $[1 + (\text{defects per unit area} \times \text{Die area})/\alpha]^{-\alpha}$

Okay here is the figure, let us say there are 7 defects localised in process. If I had a larger die size you can see not a single chip is available here, okay. Though it is randomised but the intention really this way, so that you do not actually get...

Maybe one chip out of for you got, okay. Or maybe I should have put it here, it is okay. However if I reduce the die size and kept same effects you can see that at least there will be 14 to 15 chips out of 20 odd numbers I am saving. So if you increase the wafer size, if you increase the die size, it does not really help, is that clear? Unless your processes are defect free and these are something which is not so easy to control all peoples trying their best.

So there is always a game, how big the chip size should be for example Pentium has around 1.7 5 into 1.4 centimetre first Pentium chip but they are not going beyond 2 centimetre they are not looking how 4 centimetre square chip because that is a problem. If I put larger chip size here no chip is possible, a defect everything gone, okay. Otherwise I will have full wafer as one chip system, okay.

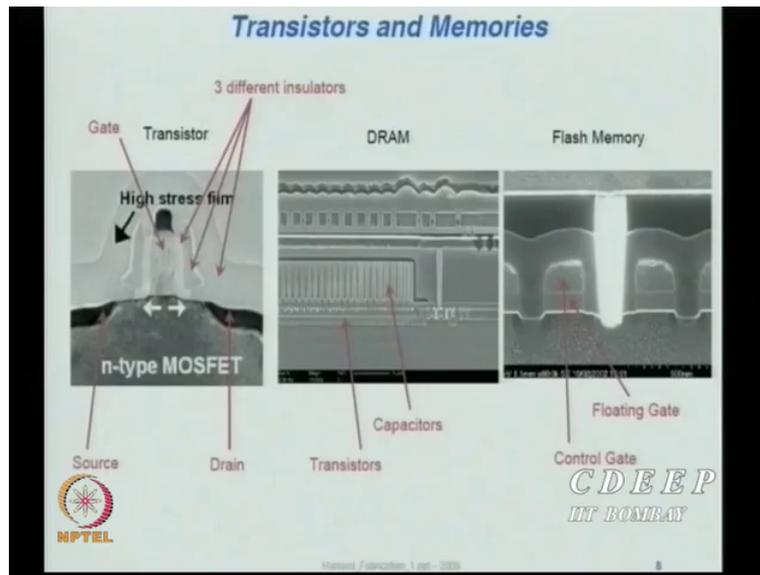
But one defect whole wafer gone, 12 inch wafer cost around 600 dollars, so it will vanish in the air. Processing cost you have done so much and also billion dollars lost or hundred thousand dollars lost. So the problem starts how good is the defect free process? One of the area which is

called manufacturability which this course may not teach you, I may not discuss I just want to tell you why processes you must learn because at the end of the day our worry is cost, okay.

So as good a process you create at that much cost to do it is and that is where the market is, okay. So why people normally go for (()) (67:44) products the memories, DRAMS, SRAM because they are sold in millions or trillions. So even if it is less yield the sale is so high, you do not mind actually wasting some money but if you are making a particular circuit for an application, how many chips will be what may be 10,000, 20,000, a lakh then the cost is so high end people may not buy this a to 50 dollars I do not want it then you will buy?

So the question and almost the due regards to all of you and myself I should keep but since this whole silicon technology is from US that money also goes in dollars we know it is changing everyday with our rupee, so I do not know what multiplier should be 60 or 58.5 or 64, the rate of the Indian currency changes every day. So I do not want that, so keep USD which is standard but that is not fair why should we look for US? But that is our life we cannot do much. So also the die cost is strong function of die area and its proportional to third or fourth power of the die area. Actually if it is very high larger dies are used.

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Before we equate these are the 3 possible technologies which VLSI people are looking for in the market. First is transistor, typical MOSFET transistor is shown here, this is of course interesting this is for single fin FET this is Intel process, this is silicon germanium and this is silicon nitride, okay. There are 3 different types of insulators used and this is a difficult transistor can be used in logic.

The second technology is called Logic technology the second is DRAM, which is the highest saleable memory chip. Where do you think DRAM is put on a desk top at any system? Where is it? Your main processor which has how many...

What memory it has? Cash, so at best L1, L2, L3, L4 maybe few kilobytes whereas we need giga, so the first memory just outside the processor which is connected as a first DRAM maybe data RAM but it is DRAM, okay. Then there is a next DRAM then hard disk, so DRAM is the highest saleable component as of now, okay. Camera every such device will require some temporary memories of high-value, okay.

And that is why this is the second technology, one is processor technology or logic based, the second is memory based it is both for DRAM as well as this RAM but most for DRAM and third technology which is taking over now because most of the problem started with as SRAM and

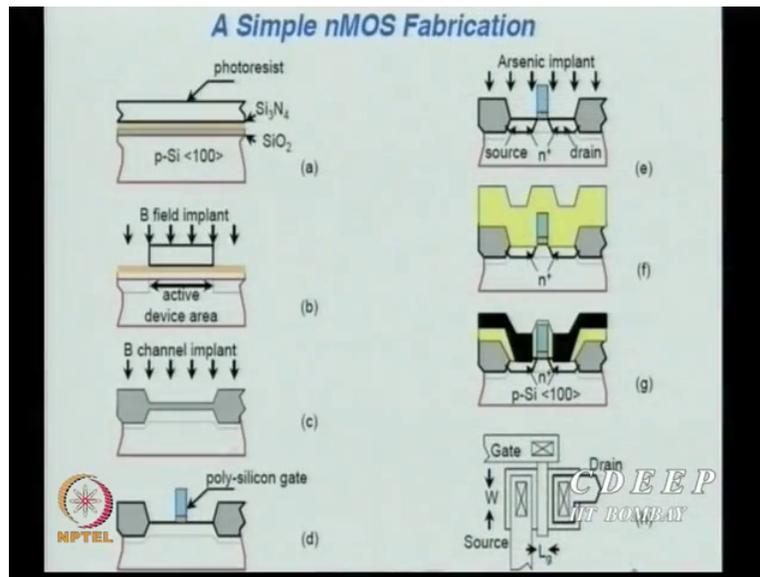
DRAM was DRAM is a dynamic, so it actually loses data after sometime of use or even otherwise.

And SRAM of course is the powered device all time, so it loses data when the power is gone away. So we came with E square prom or E proms which can be stored out without power, the problem there is you can put large amount of data on those E proms, you can directly increase the memory but then the excess time, time taken to take data out is way high then E proms or E square prom.

So the effort now as long as the best because it is very high-speed memory excess times can be few nanoseconds whereas in the case of flash it maybe milliseconds in earlier ones. Now of course they have gone to micros. So they are looking for even faster time memories and you want to erase them in one go it is called Flash. So effort right now is to make Flash memories which are closer to DRAM speed if not to SRAM speed, okay.

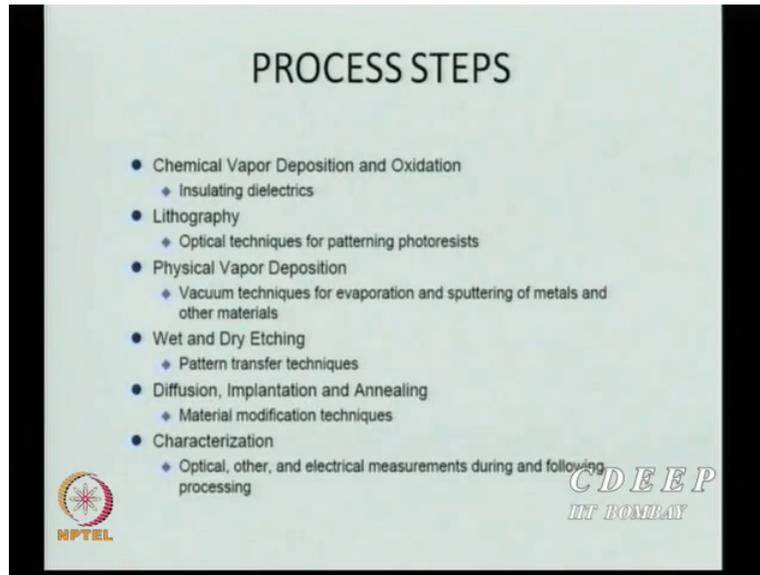
Well what is advantage? Then I do not have to power all the time and that is something great it may happen, if it happens SRAM market will go away or DRAM market may go away but this is still follows 16 years from now or 10 years from now I am not there.

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Typically this is the processing sequence maybe we will come back again and discuss but this is what it is. I will come back to it later.

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So just to give before we quit is the process steps which are the main processes which when used in this whole course are the following that you may not down. Normally we talk about short forms chemical vapor deposition is called CVD. So there will be some processes called using CVDs then there will be processes for an oxidation of silicon or any other material they are created used for insulating dielectrics, okay.

CVD and oxidation, insulating diode they create dielectrics that is silicon dioxide and nitride many other things, hafnium oxide, zirconium oxide, germanium oxide, all oxides can be deposited or by oxidised the material itself, okay. On gallium arson I cannot create silicon dioxide I will have to deposit because gallium arson is a different material. So it needs depositions and you may also need growths, okay.

If a heat silicon at around 850 and above or any other process maybe low-temperature I get silicon plus oxygen Si plus O₂ is SiO₂ and to great surprise sand, SiO₂ is sand and it is third-largest abandoned material on Earth that is why silicon will stand because material is infinite. Water and sun these are the other 2, third-largest material available on the crest of Earth is sand, okay.

And you create silicon out of this sand process is damn costly but that is what it is. The second process I have imposed which is the most important process right now which allows you

deduction in sizes, some 90 nanometres, 65, 45, 32, now these are called nodes, these numbers they came from simple idea of Moore you divide it or multiply it by 0.7, 19 to 0.7 is 63, so we say next node is 65.

65 into 0.7 is roughly 45, 45 into 0.7 is 32, so these numbers essentially are 0.7 down, okay. However this is our home work now because what was thought as a technology limit are nothing to do with this number now. 16 nanometre processes using 9 nanometres of gate oxides, okay. So there is no scaling in that order but nodes are still called back, okay. So 11th nanometre technology will have actually gate length of 7 nanometres.

7 nanometre technology may have 3 nanometres, of course 3 nanometres is worrying some because one monolayer of silicon is 5 angstrom. Now that is 0.5 nanometres, I know how do you create less than one monolayer at least one atom would be needed over there. So we do not know, so we will do something else I cannot create silicon dioxide than what else? So circuit people gave some hints, so we use that technology.

So lithography is separating the 2 lines. Generally it actually shines light, so light rolling decides how much separation because the optics has its own laws. So the minimum feature which I can separate or (()) (75:54) is essentially the limit of lithography and we are gone from optical lithography even now we are doing it to some extent. Electron beam lithography, (()) (76:03) lithography and finally ion beam lithography, so right now we are still working on optical lithography even for 16 nanometre process which has a wavelength of light use is 190 nanometres and still able to actually get your (()) (76:21) 16 nanometres which is great. We will tell you this is what lithography is all about.

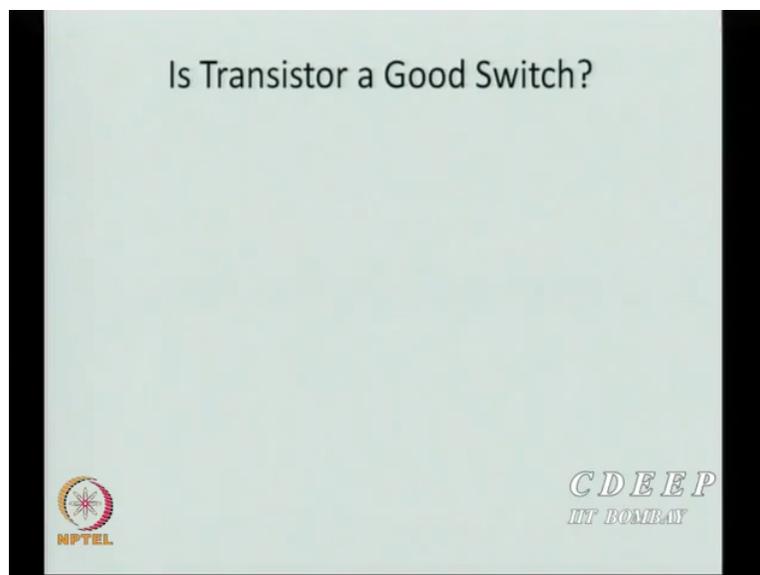
And there is PVD physical vapor deposition, you can hit the material in the vacuum either evaporate the material or sputter the material we will see things (()) (76:37) then you will have to remove certain areas to create different parts P area, N area, oxides, non-oxides, so you need to etch, so there can be solution based wet etching or dry etching by plasma, so to pattern the area.

1 there will be imperative incorporation which may be due to diffusion or implants and they will create defects you need some thermal processes called annealing which actually modifies the

material itself P channel, P device, N device or others and finally we will require many instruments for both optical as well as electrical measurements which is called characterization.

In fact IIT Bombay has the best characterization lab, the most Indian universities I IIT's, IIC's, no one has as good a characterization as we have and we believe that it is good enough because we can get devices from somewhere and can still characterize and still publish great favour, okay. Making small diode is not easy but characterize anyone else's device is relatively, because you know the process, okay.

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Okay we will come back to it later, the first question was asked is transistor a good switch and if it is not technologically what do I do? That it makes a good switch, okay. Thank you very much for the day.