

Switching Circuits and Logic Design
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Lecture – 43
Design of Registers (Part – II)

So, in the last lecture means we had started our discussion on registers and we looked at the design of parallel in parallel out registers. Now we continue with the discussion on the Design of Registers in this lecture also.

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Shift Register

- A shift register is a register in which the binary data can be stored, and the data can be shifted to the left (or right) when a shift signal is applied. 1011
→ 0101
 - New bit gets shifted in; bit shifted out typically get lost.
- Can be constructed simply by connecting D, SR or JK flip-flops in cascade.
- A 4-bit shift register is shown below: Right Shift

The diagram shows a 4-bit shift register with four D flip-flops. The Serial In (SI) is 0, and the Serial Out (SO) is 1. The CLK signal is common to all flip-flops. The Q outputs are 0, 1, 0, 1 from left to right.

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Now, in this lecture we shall specifically be talking about shift registers. Now I mentioned during the last lecture that a shift register is a register which has serial in and serial out shifting facilities.

So, let us try to understand what this serial in serial out and shifting facilities mean and how we can design a register with these facilities ok. So, talking about a shift register; a shift register is nothing but a register. Register means it can store let us say k-bit shift register will be able to store k bits of data, where binary data can be stored, but additionally you can shift the data either to the left or to the right whenever required. There is a corresponding shift signal that can be used to do that. Now what do you mean by shifting?

This I will illustrate with this example that I have shown here. Let us talk about this example, here I am showing a 4-bit shift register which is actually a right shift register; data will be shifted on the right. Let us say how it works? Look here also we have used D flip flops like a just like a PIPO register and clock as usual is been connected in parallel to all the flip flops, but the way I have applied inputs to the D inputs of the flip flops are different, the first flip flop is getting its input from an external input call serial in.

The second flip flop is getting the data input from the output of the previous; similarly the third D 3 is getting from the output Q 2, D 4 is getting from the output Q 3 and the final flip flop the output that you are calling as serial output. So, let us see that how it actually works, let us assume that the data that is stored in this register are 1 0 1 1; let us say at any particular point in time we have stored data 1 0 1 and 1 and in the external serial input I have applied the 0.

Now, a clock comes. Now understand what happens; these 0 is being fed to this input D 1 this 1 is being fed to the input D 2, this 0 is in D 3 and this 1 is in D 4. So, whenever this clock comes this data will get stored in the flip flops in parallel. So, this 0 will get stored this will become 0 this 1 will get stored, this will become 1 this 0 will get stored 0, this 1 will get stored this remains 1. So, earlier it was 1 0 1 1 it was 1 0 1 1; now this external data 0 has come, now it will becomes 0 1 0 1.

Now, you see effectively initially I had 1 0 1 1; there has being a shift to the right, this 1 has moved here 0 has moved here this 1 has moved here and some new data has being shifted in and the previous rightmost data has shifted out right. So, in this way I can apply new data's serial input once every clock and some new data can get shifted in 1 by 1 this is essentially how our shift register works. Now in this design I showed how to use a shift register using D flip flops, but you can also use JK or SR flip flops.

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Shift Register

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 - New bit gets shifted in; bit shifted out typically get lost.
- Can be constructed simply by connecting D, SR or JK flip-flops in cascade.
- A 4-bit shift register is shown below:

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Like for example; if you are using JK flip flop this will be J 2 and there will be another input K 2. So, they will be Q 1 here and K 1 bar; so, Q 1 will be connecting to J 2 and Q 1 bar will be connecting to K 2 like this the connection will be there.

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- Some shift registers have a shift enable signal *SHIFT*, which is used in the same way as the *LOAD* signal of a PIPO register.
 - Sample timing diagram is shown, assuming that the initial state is $Q_1Q_2Q_3Q_4 = 0101$.

CLK	SI	Q1	Q2	Q3	Q4
0	1	0	1	0	1
1	0	1	0	1	0
2	1	0	1	0	1
3	0	1	0	1	0
4	1	0	1	0	1

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Similarly, for SR flip flop right now there are some shift registers which have a separate shift enable signal SHIFT and just like in a PIPO register who have used a LOAD. So, either you can use a gated block or using a multiplexer I can use it. So, in a very similar way I can use that shift signal in conjunction with the clock signal to enable the shifting;

I can use the gated clock also clock and gate clock and shift I can generate the clock signal for the flip flops or that can you use that multiplexer kind of a circuit that you discussed right ok.

Now for the flip flop circuit that we have shown earlier I am showing a so called timing diagram. Now, for sequential circuits this timing diagram is very important to understand that how the things work. Here I am showing the timing diagram of a 4 bit register as the diagram you saw earlier, where have assume that the initial state of the register is 0 1 0 1. So, what I am showing in this diagram? I am showing the clock signal. Clock signal is coming continuously and this red marked edges means this is the active edge; it is rising edge triggered or the flip flops and SI is one of the inputs serial input and the 4 flip flop outputs are also shown.

So, as I said initial state is 0 1 0 1; so it is 0 1 0 and 1, let us see the when we first clock edge comes here this value of SI was 1 high. So, this 1 will get shifted in this 1 will come here, this 0 will come here, this 1 will come here; these 0 will come here. Next clock comes this 1 will come here, this previous value of Q 1 this will come here, previous value of this will come here and previous value of Q 3 will come here.

Similarly when the next clock comes here; now SI is 0. So, this 0 will come here this 1 will come here, this 1 will come here and this 0 will come here. So, there is a shifting that is going on bits are getting shifted Q 1 to Q 2 Q 2 to Q 3 Q 3 to Q 4 right.

So, this 1 this diagram whatever shown if I want to show in sequence. So, it will be like this initially the 4 outputs I am showing; initially it was 0 1 0 1. So, after the first clock it becomes 1 0 1 0, after the second clock it becomes 1 1 0 1, third clock 0 1 1 0, fourth clock 1 0 1 1. Now see there is a shifting going on you see this 0 is getting shifted like this. This 1 is getting shifted like this this 0 is getting this 1 is getting shifted like this. This is why with quality shift register this is the axis of time right. So, with time the bit cell getting shifted this is Q 1 and this is Q 4 Q 1 to Q 2; Q 2 to Q 3 Q 3 to Q 4 and finally, 1 of the bit goes out this is essentially what shift register is and this is how a simple shift register works right.

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Variations of Shift Registers

- Depending upon the way the various stages are connected, there can be various types of shift registers:
 - a) Ring counter
 - b) Twisted ring or Johnson counter
 - c) Bidirectional shift register
 - d) Universal shift register
 - e) Linear feedback shift register

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Now, there are several variations of shift registers that are possible depending on how you are connecting them ring counter, twisted ring or Johnson counter, bidirectional shift register, universal shift register and something called linear feedback shift registers. So, some of these we shall be discussing in this lecture.

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(a) Ring Counter

- This is obtained from a SISO shift register by connecting the Q output of the last flip-flop to the D input of the first flip-flop.
 - Typically, a ring counter is initialized with a single 1 and all remaining 0's.
 - This can generate multi-phase clock, or sequence of synchronizing pulses.
- For a k -bit ring counter, the contents of the register gets repeated after k clocks.
 - *Modulo- k counter.*

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Let us see first the ring counter; well the shift register circuit that you saw some time back that is essentially a serial in serial out register. Here the data are not being loaded in parallel; data is being fed serially 1 bit at a time and on the other side 1 bit at a time is

coming out. So, we call it serial in serial out data is being fed 1 bit at a time and data is also coming out 1 bit at a time.

So, this was a SISO register Serial In Serial Out; now ring counter is a special kind of SISO register where instead of applying an external serial input; SI what we do? The Q output of the last flip flop with connect to the D input of the first flip flop; so, how does it look like? This will see there are 4 stages you ; just recall there will be multiple stages of the flip flop whatever saying is that that the shift register be connected as usual.

But the output of the last stage we are feeding as the input of the first stage this is what a ring counter is actually designed like. But typically in the ring counter we will load with a single 1 and the remaining 0. Let us say 1 0 0 0 or 0 0 0 1 because if you load it with all 0. So, it will always remain 0 because this 0 will be fed back again 0 will go in, but here this 1 will cyclically rotate 1 will come here than here than here again come back. So, we shall see some typical applications of sub ring counter we can use something called a multiphase clock or some sequence of synchronizing pulses, but one thing to notice that for a k-bit ring counter.

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(a) Ring Counter

- This is obtained from a SISO shift register by connecting the *Q* output of the last flip-flop to the *D* input of the first flip-flop.
 - Typically, a ring counter is initialized with a single 1 and all remaining 0's.
 - This can generate multi-phase clock, or sequence of synchronizing pulses.
- For a *k*-bit ring counter, the contents of the register gets repeated after *k* clocks.
 - Modulo-*k* counter.

Handwritten notes on the slide:

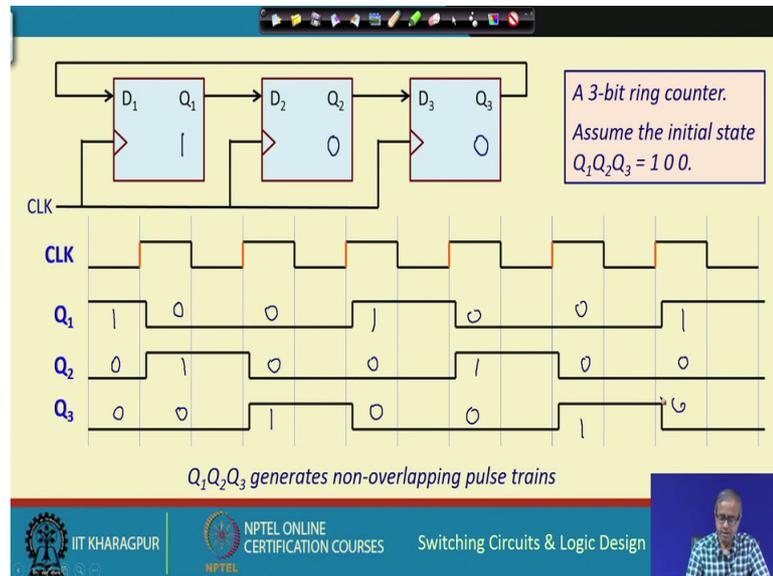
4 $\begin{bmatrix} 1000 \\ 0100 \\ 0010 \\ 0001 \\ 1000 \end{bmatrix}$ mod-4

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Let us say I have a 4 bit ring counter 1 0 0 0 ; so, after 1 clock it will become 0 1 0 0, after 2 clock it will become 0 0 1 0 after 3; 0 0 0 1 and after 4 it again becomes 1 0 0 0.

So, the sequence repeats after every 4 patterns; so we call it modulo 4 counter mod 4 counter. So, for a k-bit ring counter we can implement a modulo k counter; so, after this k number of patterns; the pattern again starts with 1 0 0 0 and repeats right.

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So, this is how a ring counter looks like; so, here I am shown the diagram of a 3 bit ring counter there are 3 flip flops the output Q_3 is connected to D_1 . And we assume that initially we will load the flip flop with 1 0 0; so this has 1, this has 0 and this has 0.

So, if you again look at the timing diagram for this see initially this was 1 1 0 0 as I said. After the first clock comes there will be a shifting 1 will come here 0 will come and this 0 will again come back here. So, this 1 we will come here 0 we will come here and this 0 will come back to Q_1 . So, 0 1 0 at the next clock this 1 will come here, 0 will be here and 0 is the here. Next clock again 1 is coming back 1 0 0, next clock this 1 again is shifting here 0 1 0 0 0 1 and again 1 0 0; this repeats right.

Now, if you look at the kind of pulses that are generated in Q_1 , Q_2 and Q_3 ; you see in Q_1 there is a pulse which is generated here right this and remaining time it is 0 for Q_2 it is here and for Q_3 it is here. So, if I consider this whole thing as my time period; then in this time period first Q_1 is active then Q_2 is active, then Q_3 is active.

So, I can say that $Q_1 Q_2 Q_3$ is generating non overlapping pulse train because $Q_1 Q_2 Q_3$ again Q_1 starts; again Q_1 again Q_2 and Q_3 . So, in many applications we need

something called multiphase clocks and using a ring counter we can very easily generate such multiphase clocks. If you need 4 phase clock use a 4 bit ring counter and apply a clock of sufficiently high frequency, you will be generating the clocks from the 4 outputs, there will be shifted in phase there will be non overlapping right.

And just another thing I did not mention you see from this time in diagram that whenever this clock edge comes; the time when this output of the flip flop is changing there is a small delay which is shown, there is a small gap right. This small gap is due to the delay of the flip flops that a value has been applied in a clock comes after sometime after how much time the output Q 2 will start changing.

So, this gap that you see for example, here this gap actually indicates that delay right. So, when you draw a timing diagram like this; this is delay should also be specified because the flip flops are not ideal flip flops, whenever you change a clock the outputs do not change immediately.

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(b) Twisted Ring or Johnson Counter

- This is obtained from a SISO shift register by connecting the Q' output of the last flip-flop to the D input of the first flip-flop.
 - The Johnson counter can be initialized to the all-0 state.
 - The 0's and 1's are consecutive in the generated patterns (may be required for some applications).
- For a k -bit Johnson counter, the contents of the register gets repeated after $2k$ clocks.
 - Modulo- $2k$ counter.

Handwritten notes: 4-bit, 8 unique patterns

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There is a small delay after which the outputs change ok; so this is how a ring counter works. Next let us come to a very small variation of a ring counter; this is called a twisted ring or a Johnson counter. Now in a ring counter what we did? The Q output of the last flip flop, we fed to the D input of the first flip flop. Now in a Johnson counter what you do? We take the Q bar output of the last flip flop. And that Q bar I feedback to

the D input of the first flip flop this is the only change this is called twisted ring or a Johnson counter.

So, as I mentioned it is specified here; we connect the Q bar output of the last flip flop to the D input of the first flip flop. And in a Johnson counter you can very easily initialize it to the all 0 state I means unlike a ring counter; in a ring counter if initialize it to the all 0 state; it will always remain in the all 0 state because none of the flip flops can become 1, but here it can become.

And you will see that in a Johnson counter the kind of patterns that are generated 0s and 1s are consecutive, which may be useful in some applications. And another feature is that for a k-bit Johnson counter I mean it counts modulo 2k like; let us say for a 4 bit Johnson counter it will generate 8 unique patterns before repeating twice of k right. So, this I will I mean illustrating with an example.

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Clocks	1	2	3	4	5	6	7	8	9
Q_1	0	1	1	1	0	0	0	0	...
Q_2	0	0	1	1	1	0	0	0	...
Q_3	0	0	0	1	1	1	0	0	...
Q_4	0	0	0	0	1	1	1	0	...

A 4-bit Johnson counter.
Assume the initial state $Q_1Q_2Q_3Q_4 = 0000$.

Let us take a 4 bit Johnson counter as I have shown here, there are 4 flip flops as you can see I have connected the Q bar of the last flip flop to the D input of the first flip flop. And I am showing in the sequence of time the clock pulses what is happening.

And I am assuming that the initial state is all 0. So, in this table I means; so, initially the outputs are all 0s; so 0 0 0 0. Now just the only thing to remember is that the bar of the

last bit will be fed to the first bit D₁. So, after 1 clock pulse Q₄ was 0; so 1 was fed back, so this will become 1 other zeros will be shifted 0 0 0.

Second clock pulse again this bit was 0; so, not of that this 1 will be fed here, this 1 will get shifted this 1 will shift 0 0 this will be shifting. Similarly the third clock pulse this is again 0; so 1 will be fed and this bits will all be shifting. Fourth clock pulse again it was 0 ; so, again 1 will be fed shifting.

Now, the last bit is 1 ; so now 0 will be fed shifting again 1, again 0 is fed, again 1 again 0 is fed, again 1 again 0 is fed and you finally, land up again to the all 0 state. So, you see there are 8 unique states that are there 8 unique patterns which are followed; starting from the 0 1 2 3 4 5 6 7 8 0 up the 7 before it repeats again right.

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A 4-bit Johnson counter.
Assume the initial state $Q_1Q_2Q_3Q_4 = 0000$.

So, this is something you have to remember that for a Johnson counter if we have a k-bit Johnson counter as it said; there will be 2 K unique patterns that you can generate. Now there is another point that 1s and 0s are consecutive if you look at any 1 of the output let us say Q₂. So, the patterns that are generated I am looking at one side you see you see all the 1s are consecutive that together.

The 0s will be consecutive again there will be 1s, again there will be 0. So, the block of 1s and 0s are all consecutive. So, in a cycle say starting from here upto 7 you see ones

are all consecutive; there are 4 ones there all consecutive this is the property of Johnson counter right.

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(c) Bidirectional Shift Register

- Based on a control input, the shift register works in either the shift-right or the shift-left modes.
- Multiplexers are used to feed the appropriate signals to the D inputs of the flip-flops.
 - A control input L/R' selects the multiplexer inputs.
 - Determines whether to shift left or to shift right.

The slide contains two hand-drawn diagrams. The left diagram shows four flip-flops connected in a chain for left shifting, with arrows indicating the signal path from right to left. The right diagram shows four flip-flops connected in a chain for right shifting, with arrows indicating the signal path from left to right. The slide footer includes logos for IIT KHARAGPUR, NPTEL ONLINE CERTIFICATION COURSES, and the course title 'Switching Circuits & Logic Design'.

Let us now look at a more flexible kind of a shift register bidirectional shift register. See earlier the shift register circuit that we saw it was a right shift register. So, the idea was something like this there are 4 flip flops ; so, we connected the output of this to the input of this, output of this to the input of this, output of this to the input of this; so it was a right shift register.

But if I want to implement a left shift register what do I do? For implementing a left shift register the output of this one should be fed to the input of this, output of this one should be fed to the input of this, output of this one should be fed to the input of this and output of this 1 will be the final output. So, this will be shifting depth; this bit will go here, this bit will go here, this bit will go here.

So, we will have to connect the Q and Ds in the reverse order right. So, essentially the requirement is this ; so we need to use multiplexers so that the proper inputs are applied to the D and I am assuming that there is a separate control input called LR bar.

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(c) Bidirectional Shift Register

- Based on a control input, the shift register works in either the shift-right or the shift-left modes.
- Multiplexers are used to feed the appropriate signals to the D inputs of the flip-flops.
 - A control input L/R' selects the multiplexer inputs.
 - Determines whether to shift left or to shift right.

$L/R' = 1$ left
 $L/R' = 0$ right



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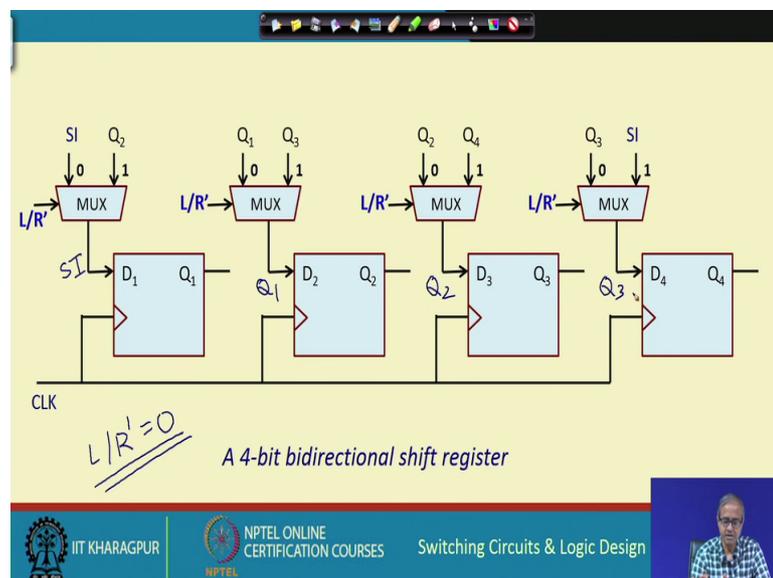
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LR bar which if it is 1; it means left shift if it is 0 it means right shift. So, let us see how the design looks like.

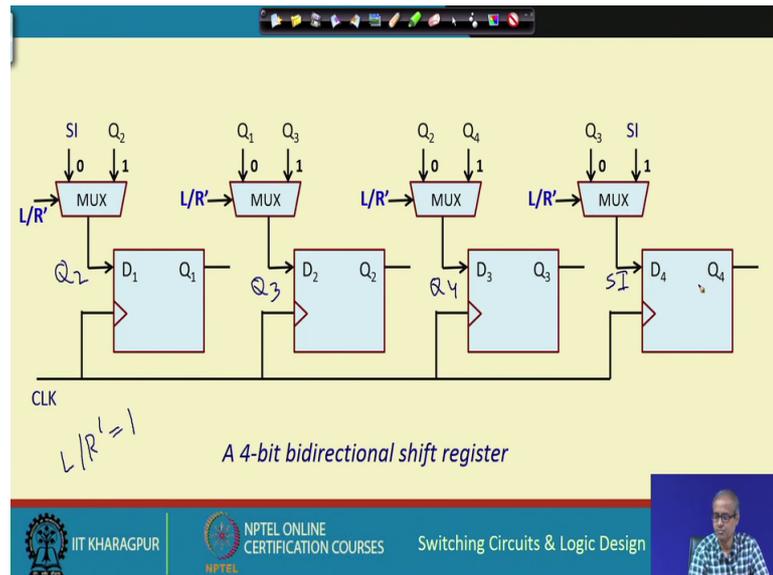
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This is the design of the bidirectional shift register; let us see there are 4 flip flops just like a normal register. Now I have not connected Q 1 to D 2 or Q 2 to D 3 directly rather there are 4 multiplexer I am using; just see all this multiplexers are having this LR bar as this select input and I have suitably apply the inputs to the multiplexer.

Let us assume I am trying to do a right shift which means LR bar is 0 right shift means this 0 inputs are selected of the multiplexer. So, this SI will come here, the SI will be coming here Q 1 will come here Q 1 will come here Q 2 will be here and Q 3 will be here. This is just like how we connected the register earlier right Q 1 was connected here, Q 2 was here and Q 3 was here this is normal right shift.

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But if you want to do left shift then my LR bar would be 1. Now if my LR bar will be 1; let us see what will happening, now it will start from the right side. So, my SI will be coming here because my data will now be fed to the rightmost Q 4 is coming here just like I showed, Q 3 is coming here and Q 2 is coming here.

So, shifting will be shifting will happening the reverse direction; Q 4 to Q 4 will be coming here, Q 3 will be coming here, Q 2 will be coming and Q 1 will get lost and new value will be entering in Q 4 right. So, this is how a bidirectional shift register can be designed; a normal register where the inputs to D 1 are properly selected by using multiplexers under the control of this LR bar ok.

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(d) Universal Shift Register

- A universal shift register is a bidirectional shift register, whose input can be either in serial form or in parallel form, and whose output can also be either in serial form or in parallel form.

Control Inputs		Action
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

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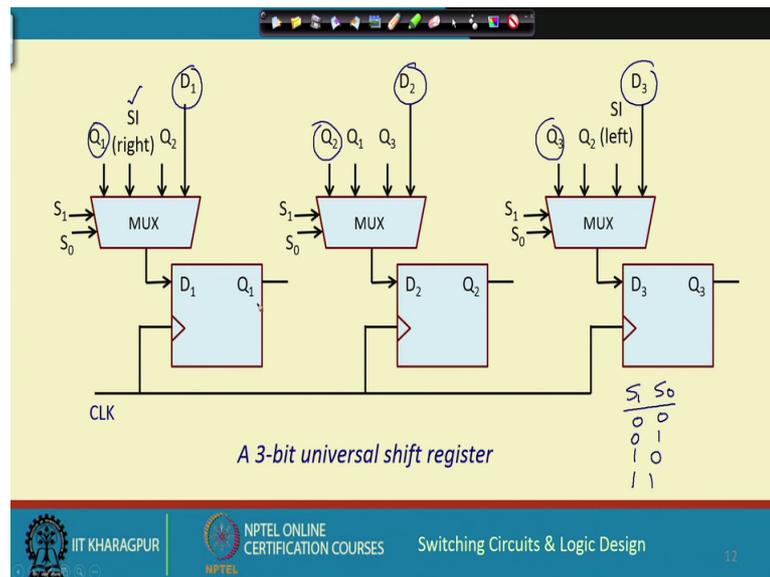
Now, the last kind of shift register that you talk about today in this lecture is a universal shift register. So, universal shift register has some added functionality; so it is a bidirectional shift register plus something more. So, what is more? What I am saying that the inputs that we are applying can be either in serial form or it can also be in parallel form and also the outputs.

Like an universal shift register looks like this; there are serial inputs available right shift left shift there can be 2 separate serial inputs. But in addition you can also parallelly load the data; now in the shift register circuits that we have seen. So, far there were no parallel data inputs that were there. Now in this universal register facility for parallel data input and also parallel data output both are also available.

So, there is a D input which can be fed from outside and there is a there is a Q output that is available from outside. But for loading you see there is no separate load control line rather there are 2 control signals S 1 and S 0.

Now, I can use these are this S 1 S 0 combinations I am showing, this is S 1 and S 0. So, if there are 0 0 it means there is no change 0 1 means right shift, 1 0 means left shift, 1 1 means parallel load. So, I can load it parallel I can do a shift left I can do a shift right and the output is also available anyway. So, let us see how I can implement this; this can be designed in a similar way in a way similar to a bidirectional shift register.

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But we need bigger multiplexers; there are 4 modes to be selected. So, I need to use a 4 to 1 multiplexer. So, you recall the multiplexer controls this S_1 and S_0 ; they were like this 0 0 means no change. So, for the 0 input the first one is the 0 input, this Q_1 I am connecting here, Q_2 I am connecting here, Q_3 I am connecting here. So, the same value is getting stored no change.

0 1 means shift right. So, for 0 1 this shift serial input right is being fed here, Q_1 is fed here, Q_2 is fed here it is just like a serial shift right and 1 0 means serial shift left. Here serial input left is fed here, Q_3 is fed here, Q_2 is fed here this is shift left and 1 1 is parallel load. You see D_1 is fed here, D_2 is fed here, D_3 is fed from outside data will get stored. So, this is how you can design for universal shift register; well an universal shift register is the circuit using which you can do all the kind of register operations; parallel load, serial input, serial output everything.

But in some specific application you may be needing just a PIPO register or shift simple shift register. So, you do not need all this multiplexers; so, if you really need then you need to have this kind of a complex universal shift register right. So, with this we come to the end of this lecture.

So, in this lecture we talked about shift registers and the various different types of shift registers that are useful in some applications like ring counter, Johnson counter then the bidirectional shift register and the universal shift register. So, we shall be continuing with

our discussion in the next lecture where we shall be talking about fifth type of shift register called linear feedback shift register. And also we shall discuss some of the practical applications of this registers and shift registers.

Thank you.