

NPTEL Video Lecture Topic List - Created by LinuXpert Systems, Chennai

NPTEL Video Course - Electronics and Communication Engineering - NOC:Design and Analysis of VLSI Subsystems

Subject Co-ordinator - Prof. Madhav Rao

Co-ordinating Institute - IIT - Madras

Sub-Titles - Available / Unavailable | MP3 Audio Lectures - Available / Unavailable

Lecture 1 - Understanding Silicon
Lecture 2 - Introduction to NMOS
Lecture 3 - NMOS Transistor Working
Lecture 4 - PMOS Transistor
Lecture 5 - MOS Capacitances
Lecture 6 - Non Ideal MOS model
Lecture 7 - Short channel current model
Lecture 8 - Short channel current model analysis
Lecture 9 - Channel Length modulation index
Lecture 10 - DC characteristics of Inverter
Lecture 11 - Transfer characteristics of Inverter
Lecture 12 - Skewed Inverter
Lecture 13 - Skewed Inverter and threshold voltage
Lecture 14 - Equivalent of transistors in series
Lecture 15 - Transmission Gate
Lecture 16 - Bad CMOS Buffer - Part 1
Lecture 17 - Bad CMOS Buffer - Part 2
Lecture 18 - Noise margin characteristics of inverter
Lecture 19 - Noise margin parameters
Lecture 20 - Introduction to Delay in CMOS
Lecture 21 - Transient analysis of CMOS Inverter
Lecture 22 - RC approximated delay
Lecture 23 - Switching Resistance
Lecture 24 - CMOS Inverter approximated to RC Circuit
Lecture 25 - Elmore delay
Lecture 26 - Delay of FO4 inverter
Lecture 27 - Extracting capacitances of 3-Nand gate for delay estimation
Lecture 28 - Characterizing Delay of NOR gate
Lecture 29 - Linear Delay model

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- Lecture 30 - Logical effort and Parasitic delay
- Lecture 31 - Logical effort and Parasitic delay for different gates
- Lecture 32 - Logical effort for short-channel current model
- Lecture 33 - Ring Oscillator design
- Lecture 34 - Optimizing Gate Size
- Lecture 35 - Optimizing Gate Sizes Example
- Lecture 36 - Optimizing the Stages for an inverter path
- Lecture 37 - Optimizing the Stages for a General Circuit
- Lecture 38 - Decoder Design
- Lecture 39 - Introduction to Combinational Circuit and assymmetric gates
- Lecture 40 - Assymmetric Gates analysis
- Lecture 41 - Assymmetric Gates analysis using short-channel current model
- Lecture 42 - Introduction to Skewed gates
- Lecture 43 - Skewed gates and best P/N ratio
- Lecture 44 - vIntroduction to Pseudo NMOS
- Lecture 45 - Psudeo NMOS gates
- Lecture 46 - Other Logic Family
- Lecture 47 - Dynamic Logic and Domino logic
- Lecture 48 - Domino gates
- Lecture 49 - Introduction to Stick Diagram
- Lecture 50 - Stick Diagram for different gates
- Lecture 51 - Applying Eulers path for stick diagram representations
- Lecture 52 - Multiplexer design and layout
- Lecture 53 - Introduction to Interconnects
- Lecture 54 - Interconnects - RC delay, and Energy
- Lecture 55 - Introduction to crosstalks in interconnects
- Lecture 56 - Transient analysis in Crosstalk
- Lecture 57 - Introduction to Repeaters in Interconnect Engineering
- Lecture 58 - Repeater Design
- Lecture 59 - Energy and delay analysis for interconnectwith repeaters
- Lecture 60
- Lecture 61 - Introduction to Power
- Lecture 62 - Switching Power and Energy Estimation
- Lecture 63 - Activity factor and estimating dynamic power for a combinational circuit design
- Lecture 64 - Analyzing Dynamic Power
- Lecture 65 - Energy estimation through driving factor
- Lecture 66 - Energy expression in terms of delay
- Lecture 67 - Voltage Scaling
- Lecture 68 - DVFS

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- Lecture 69 - Introduction to subthreshold leakage current model
- Lecture 70 - Subthreshold leakage current and Gate leakage current
- Lecture 71 - Estimating Static Power
- Lecture 72 - Introduction to CMOS Latch design
- Lecture 73 - CMOS Latch Design
- Lecture 74 - CMOS Latch and flipflop design
- Lecture 75 - Static Timing Analysis
- Lecture 76 - Static Timing Analysis (Continued...)
- Lecture 77 - Static Timing Analysis - Part 2
- Lecture 78 - Static Timing Analysis - Part 2.1
- Lecture 79 - Static Timing Analysis - Part 3
- Lecture 80 - TPDQ and TPCQ
- Lecture 81 - Static Timing Analysis - Part 4
- Lecture 82 - Static Timing Analysis - Part 5
- Lecture 83 - Static Timing Analysis - Part 6
- Lecture 84 - SET and CLEAR enabled Latch and Flipflop Design
- Lecture 85 - 1-bit Adder design
- Lecture 86 - Adder-Part2
- Lecture 87 - PG architecture - Part 1
- Lecture 88 - PG architecture - Part 2
- Lecture 89 - Carry Skip Adder
- Lecture 90 - Carry Look Ahead and Carry Increment Adder
- Lecture 91 - Other Adder Subsystems
- Lecture 92 - Approximate Multipliers - Part 1
- Lecture 93 - Approximate Multipliers - Part 2
- Lecture 94 - Approximate Adder