

NPTEL Video Lecture Topic List - Created by LinuXpert Systems, Chennai

NPTEL Video Course - Electrical Engineering - NOC:Digital System Design

Subject Co-ordinator - Prof. Neeraj Goel

Co-ordinating Institute - IIT - Ropar

Sub-Titles - Available / Unavailable | MP3 Audio Lectures - Available / Unavailable

Lecture 1 - Introduction
Lecture 2 - Analog vs Digital
Lecture 3 - Binary number system - 1
Lecture 4 - Binary number system - 2
Lecture 5 - Negative number representation - 1
Lecture 6 - Negative number representation - 2
Lecture 7 - Other number systems
Lecture 8 - Floating point numbers - 1
Lecture 9 - Floating point numbers - 2
Lecture 10 - Floating point numbers - 3
Lecture 11 - Floating point numbers - 4
Lecture 12 - Floating point numbers - 5
Lecture 13 - Boolean functions
Lecture 14 - Boolean Algebra
Lecture 15 - SOP and POS Representation
Lecture 16 - Algebraic simplifications
Lecture 17 - Canonical form
Lecture 18 - Boolean minimization using K-Maps
Lecture 19 - More Logic gates
Lecture 20 - Hardware description language:Verilog
Lecture 21 - Verilog simulation demo
Lecture 22 - K-maps
Lecture 23 - QM-method
Lecture 24 - Area delay model
Lecture 25 - Multi-level logic
Lecture 26 - Multiplexer
Lecture 27 - Four state logic
Lecture 28 - Decoders - 1
Lecture 29 - Decoders - 2

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Lecture 30 - Encoders
Lecture 31 - Programmable hardware
Lecture 32 - Ripple carry adder
Lecture 33 - Carry look ahead adder
Lecture 34 - Modeling BUS in Verilog
Lecture 35 - Fast adder: Carry select adder
Lecture 36 - Multiple operand adder
Lecture 37 - Multiplication
Lecture 38 - Iterative circuits - 1
Lecture 39 - Iterative circuits - 2
Lecture 40 - Introduction to sequential circuits
Lecture 41 - Latches
Lecture 42 - D-Flip-flops
Lecture 43 - More Flip-flops
Lecture 44 - Counters
Lecture 45 - Verilog-Behavior model - 1
Lecture 46 - Verilog-Behavior model - 2
Lecture 47 - Registers - 1
Lecture 48 - Registers - 2
Lecture 49 - Memory
Lecture 50 - Sequential circuit analysis
Lecture 51 - Derivation state graph
Lecture 52 - Sequence detector: Example 1
Lecture 53 - Sequence detector: Example 2
Lecture 54 - State machine reduction
Lecture 55 - State encoding
Lecture 56 - Multi-cycle adder design
Lecture 57 - Pipelined adder design
Lecture 58 - Multiplication design
Lecture 59 - Division hardware design
Lecture 60 - Interacting state machines
Lecture 61 - Register Transfer Level design
Lecture 62 - GCD computer at RTL Level
Lecture 63 - RTL Design - Bubble sort
Lecture 64 - RTL Design - Traffic light controller
Lecture 65 - FPGA
Lecture 66 - Xilinx CLB
Lecture 67 - FPGA - Design flow
Lecture 68 - FPGA design demo

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Lecture 69 - Introduction to ASIC design flow - Part 1
Lecture 70 - Introduction to ASIC design flow - Part 2
Lecture 71 - Future directions