

NPTEL Video Lecture Topic List - Created by LinuXpert Systems, Chennai

NPTEL Video Course - Electrical Engineering - NOC:Digital IC Design

Subject Co-ordinator - Prof. Janakiraman

Co-ordinating Institute - IIT - Madras

Sub-Titles - Available / Unavailable | MP3 Audio Lectures - Available / Unavailable

Lecture 1 - Introduction - Digital IC Design
Lecture 2 - PN Junction
Lecture 3 - MOS Capacitor Threshold Voltage
Lecture 4 - MOS Transistor Current Expression
Lecture 5 - Body Effect and I-V Plots
Lecture 6 - Short Channel Transistors - Channel Length Modulation
Lecture 7 - Velocity Saturation and Level-1 SPICE Model
Lecture 8 - Drain Induced Barrier Lowering
Lecture 9 - Sub-Threshold Leakage
Lecture 10 - Substrate and Gate Leakage
Lecture 11 - The PMOS Transistor
Lecture 12 - Transistor Capacitance - 1
Lecture 13 - Transistor Capacitance - 2
Lecture 14 - CMOS Inverter Construction
Lecture 15 - Voltage Transfer Characteristics
Lecture 16 - Load Line Analysis
Lecture 17 - Trip Point for Short Channel Device Inverter
Lecture 18 - Trip Point for Long Channel Device Inverter
Lecture 19 - Noise Margin Analysis - 1
Lecture 20 - Noise Margin Analysis - 2
Lecture 21 - Noise Margin Analysis - 3
Lecture 22 - Noise Margin Analysis-Long Channel Device Inverter - 1
Lecture 23 - Noise Margin Analysis-Long Channel Device Inverter - 2
Lecture 24 - Pass Transistors
Lecture 25 - NMOS Transistor ON Resistance and Fall Delay
Lecture 26 - Elmore Delay Model
Lecture 27 - Inverter: Transient Response
Lecture 28 - Inverter: Dynamic Power
Lecture 29 - Inverter: Short Circuit Power

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- Lecture 30 - Inverter: Leakage Power and Transistor Stacks
- Lecture 31 - Stacking Effect and Sleep Transistors
- Lecture 32 - Ring Oscillators and Process Variations
- Lecture 33 - Implementing Any Boolean Logic Function
- Lecture 34 - Implementing Any Boolean Logic Function: Examples. Gate sizing
- Lecture 35 - Gate Sizing
- Lecture 36 - Logic Gate Capacitance
- Lecture 37 - Gate Delay
- Lecture 38 - Parasitic Delay
- Lecture 39 - Gate Delay with a Load Capacitance
- Lecture 40 - Logical Effort
- Lecture 41 - Gate Delay
- Lecture 42 - Path Delay Calculation and Optimization Formulation
- Lecture 43 - Path Delay Optimization: Intuition
- Lecture 44 - Path Delay Optimization: Example
- Lecture 45 - Buffer Insertion
- Lecture 46 - Input Ordering and Asymmetric Gates
- Lecture 47 - Skewed Gates
- Lecture 48 - Special Functions
- Lecture 49 - Pseudo NMOS Logic
- Lecture 50 - Pseudo NMOS Inverter
- Lecture 51 - Pseudo NMOS Logical Effort and CVSL
- Lecture 52 - Dynamic Circuits and Input Monotonicity
- Lecture 53 - Domino Logic and Weak Keepers
- Lecture 54 - Transmission Gate Logic
- Lecture 55 - Gate Sizing for Large Circuits
- Lecture 56 - Ripple Adder Introduction
- Lecture 57 - Full Adder Circuit Implementation
- Lecture 58 - Full Adder Optimization
- Lecture 59 - Carry Skip Adder
- Lecture 60 - Carry Select Adder
- Lecture 61 - Linear and Square Root Carry Select Adder
- Lecture 62 - Two's Complement Arithmetic
- Lecture 63 - Two's Complement Sign Extension
- Lecture 64 - Array Multiplier
- Lecture 65 - Array Multiplier - Timing Analysis
- Lecture 66 - Carry Save Multiplier
- Lecture 67 - Carry Save Multiplier - Signed Multiplication
- Lecture 68 - Introduction to Pipelining

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- Lecture 69 - Time Borrowing
- Lecture 70 - Master Slave Flip Flop
- Lecture 71 - Flop Timing Parameters
- Lecture 72 - Alternate Circuit Implementations
- Lecture 73 - Clock Overlap
- Lecture 74 - C2MOS Flop
- Lecture 75 - Flop Characterization
- Lecture 76 - Max and Min Delay of Flop Based Systems
- Lecture 77 - Flop Min Delay Constraint
- Lecture 78 - Latch - Max and Min Delay Constraints
- Lecture 79 - Latch - Timing Analysis with Skew
- Lecture 80 - Time Borrowing