NPTEL Video Course - Electrical Engineering - NOC:System Design through VERILOG

Subject Co-ordinator - Prof. Shaik Rafi Ahamed

Co-ordinating Institute - IIT - Guwahati

Sub-Titles - Available / Unavailable | MP3 Audio Lectures - Available / Unavailable

Lecture 1 - Verilog Operators and Modules
Lecture 2 - Verilog Ports, Data types and Assignments
Lecture 3 - Basics of gate level modeling
Lecture 4 - Half adder, full adder and ripple carry adder
Lecture 5 - Parallel adder/subtractor
Lecture 6 - Multiplier and comparator
Lecture 7 - Decoder, encoder and multiplexer
Lecture 8 - Demultiplexer, read only memory
Lecture 9 - Review of flip-flops
Lecture 10 - Verilog modeling of flip-flops
Lecture 11 - Modeling of CMOS gates and Boolean functions
Lecture 12 - Modeling using transmission gates, CMOS dalay times
Lecture 13 - Signal strengths
Lecture 14 - Basics of dataflow modeling
Lecture 15 - Examples of dataflow modeling
Lecture 16 - Basics of behavioral modeling
Lecture 17 - Examples of behavioral modeling
Lecture 18 - Verilog modeling of counters
Lecture 19 - Verilog modeling of sequence detector
Lecture 20 - Verilog modeling FSMs and shift registers
Lecture 21 - Combinational circuit examples
Lecture 22 - Sequential circuit examples
Lecture 23 - Arithmetic and Logic Unit (ALU)
Lecture 24 - Static RAM and Braun Multiplier
Lecture 25 - FIR filter implementation
Lecture 26 - Baugh-Wooley signed multiplier architecture
Lecture 27 - IIR filter implementation

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